RELIABLE MINIATURE SPACEBORNE MEMORY

Interim Engineering Report

November 19, 1964 Through July 26, 1965

Contract No. NAS5-9518

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland

UNIVAC
DIVISION OF SPERRY RAND CORPORATION
P.O. BOX 500 · BLUE BELL, PENNSYLVANIA

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Abstract

This report presents the results of work done during the 8-month design phase (Phase I) of an 18-month contract to design and build an engineering model of a miniature spaceborne memory. The memory system which has been designed has the following characteristics:

Memory Element	Magnetic, thin film, plated-wire.
Storage Capacity	2,949,120 bits.
Speed	500-kilocycle serial bit rate. 125-kilocycle 4-bit character rate.
Organization	Two independent half-memories of 1,474,560 bits permit simultaneous reading and writing.
Operating Mode	Nondestructive readout, serially addressed buffer memories.
Input Voltage	$-24.5 \pm 2\%$ volts.
Input Power	0.5 watt - Standby (design objective). 1.5 watt - Continuous 500-kilocycle writing (design objective).
Temperature Range	Operating, -20°C to $+80^{\circ}$C. Storage, $+150^{\circ}$C for 48 hours.
Memory Stack	The 1,474,560 bits of memory, 2592 diodes, and 96 transistors associated with the memory stack fit into a space 6 inches by 13 inches by 2.2 inches including an external case.

Foreword

This report describes work performed during the 8-month phase I of the 18-month contract NAS5-9518 for a Reliable Miniature Spaceborne Memory. This contract with the UNIVAC Division of Sperry Rand Corporation, P. O. Box 500, Blue Bell, Pa., has been directed by Mr. A. Whitehead and Mrs. M. Townsend, NASA Goddard Space Flight Center Technical Officer.

The work is being performed under the supervision of Mr. G. A. Fedde, Engineering Manager of the Advanced Memory Development Laboratory. Mr. W. J. Bartik, Manager of the Advanced Electronics Section, provides technical consultation and general management of the contract. The following persons are assigned directly to the project and, along with others, have made valuable contributions: E. N. Schwartz, R. Mosenkis, C. A. Nelson, and A. L. Salamon of the Advanced Memory Development Laboratory; Dr. J. S. Mathias and F. J. Hanson of the Materials & Processes Research Laboratory; G. R. Reid and R. W. Hoffman of the Advanced Packaging Laboratory; and P. C. Candelori and R. A. Grossman of the Reliability & Engineering Laboratory.

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SECTION 1

INTRODUCTION

The objective of this contract is to design a 2.8 x 10^6-bit Miniature Spaceborne Memory System. This memory design can be described by the following characteristics:

Storage capacity	2,949,120 bits.
Information bit rate	500 kilocycles, serial bit rate. 125 kilocycles, 4-bit character rate.
Addressing	Sequential, first-in first-out.
Operating mode	Nondestructive readout, serially addressed buffer memories.
Organization	Two independent half-memories of 1,474,560 bits permit simultaneous reading and writing.
Input power	0.5 watt - Standby (design objective). 1.5 watt - Continuous 500-kilocycle writing (design objective).
Temperature range	Operating, -20°C to +80°C. Storage, +150°C for 48 hours.

During eight-month phase I of this contract, the design of this memory system and the low power circuits has been completed. Breadboard versions of the circuits and memory plane have been operated and tested.

The memory element used in this design is the UNIVAC-developed magnetic thin-film plated wire. The characteristics of this memory element that make it well suited for this application are:

1. Very low switching energy.
2. Very short switching time.
3. Nondestructive readout.
4. High Curie temperature, +550°C or higher.

5. Very compact, 1500 bits per square inch.

During the ten-month phase II of this contract, which started July 26, 1965, an engineering model of a half-memory will be built, tested and demonstrated. It will be shown that a prototype of such a memory could be fitted into a Nimbus box that is 4 inches by 6 inches by 13 inches.

Section 2 of this interim report describes the memory interface with external equipment, and the internal organization of the memory that was used to achieve the goals of the project. This section also includes a description of the timing and control circuits operation and the results of some approximate reliability calculations.

Section 3 contains a brief description of all of the circuits designed during phase I. A detailed report on each circuit is contained in Appendix I.

Section 4 describes the plated-wire memory element, the operation, and various tests performed preliminary to the writing of a test specification. The results of life tests on the wire are also included.

Section 5 describes the design, construction, and materials used in the memory planes and stack.

Section 6 contains the "new technology" report.

The rest of the appendices contain parts lists, hybrid circuit and semiconductor specifications, information about corrosion protection of plated wires, and information about the materials used in construction of the memory.

SECTION 2

MEMORY SYSTEM ORGANIZATION

The design of this 2.8 x 10^6-bit memory system has concentrated on achieving the lowest possible power consumption by optimizing the organization through use of lowest power circuits. Circuits operating at high repetition rates and using short rise time pulses necessarily consume more power than slower circuits. The information under the following headings shows that the processing of 40 bits in parallel every 80 microseconds to provide 1 bit serially every 2 microseconds at the memory interface yields minimum power consumption.

2.1. INTERFACE WITH EXTERNAL EQUIPMENT

The memory system accepts data or provides data output, serial by bit, at any interval 2 microseconds or longer. The data is NRZ (non return to zero) in format and is defined by the voltage level on the data lines during a clock pulse. During readout, the memory system generates a readout clock pulse to serve this function.

Zero	0.0v ±0.5v
One	+2.5v ±0.5v
Clock pulse	+2.5v ±0.5v
Read command	0.0v ±0.5v
Write command	+2.5v ±0.5v

The 2.8 x 10^6-bit memory has been designed as two completely independent half-memories. It is possible therefore to do both writing into and reading out of the memory simultaneously. In addition, the memory design permits the handling of four-bit-parallel characters at the interface. This is accomplished by elimination of the four-stage buffer counter and providing four data lines to feed data to the four-stage buffer register. Figure 2-1 is a simplified block diagram of the 1.4 x 10^6-bit half memory. In this operating mode one 4-bit character can be handled every 8 microseconds or longer.

The memory system sequentially stores and reads out the data in the same order in which it was written. Each time the state of the command line changes from read to write or vice versa, the memory address counters are reset to the first memory address. Data readout is nondestructive, and the

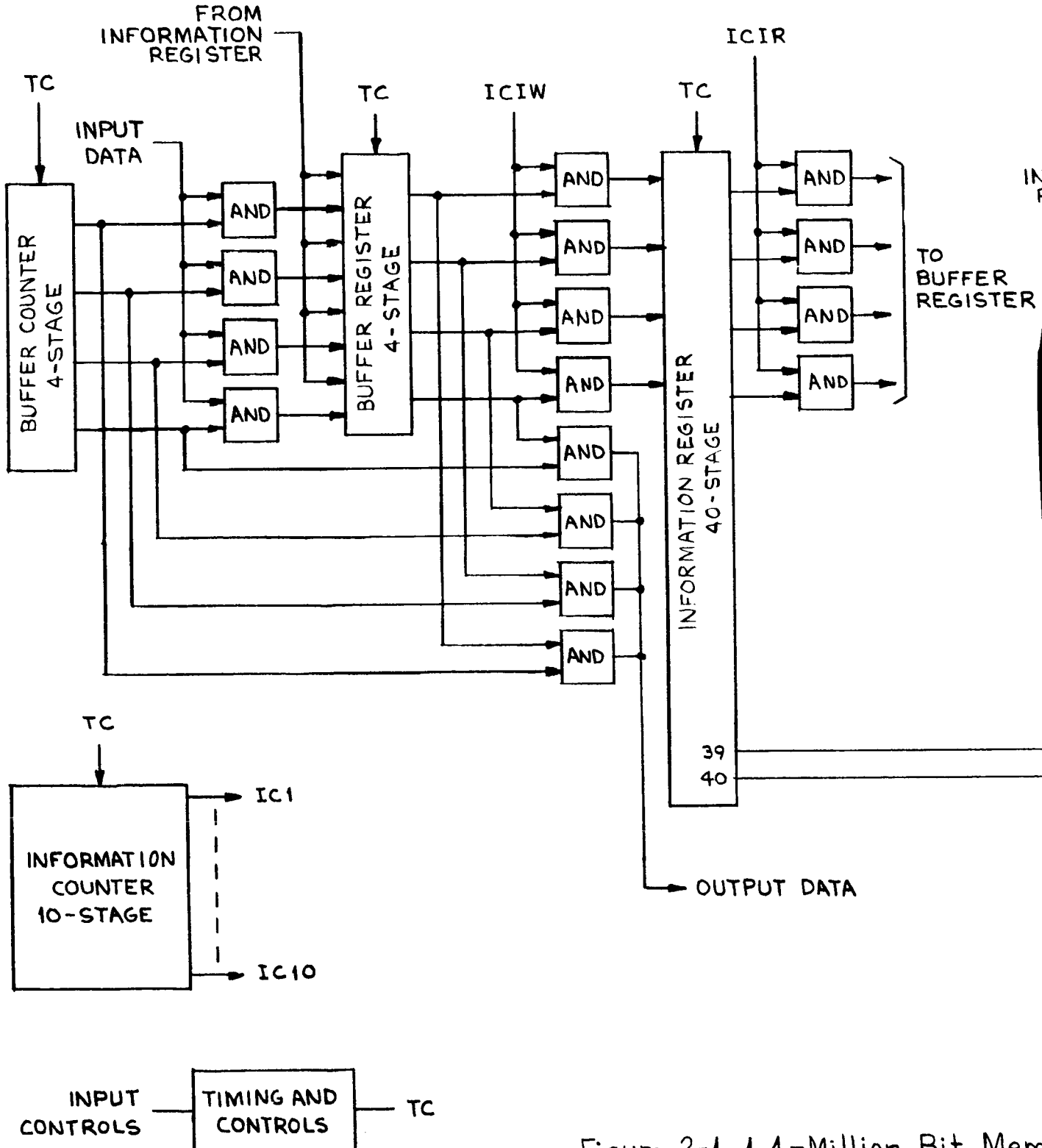
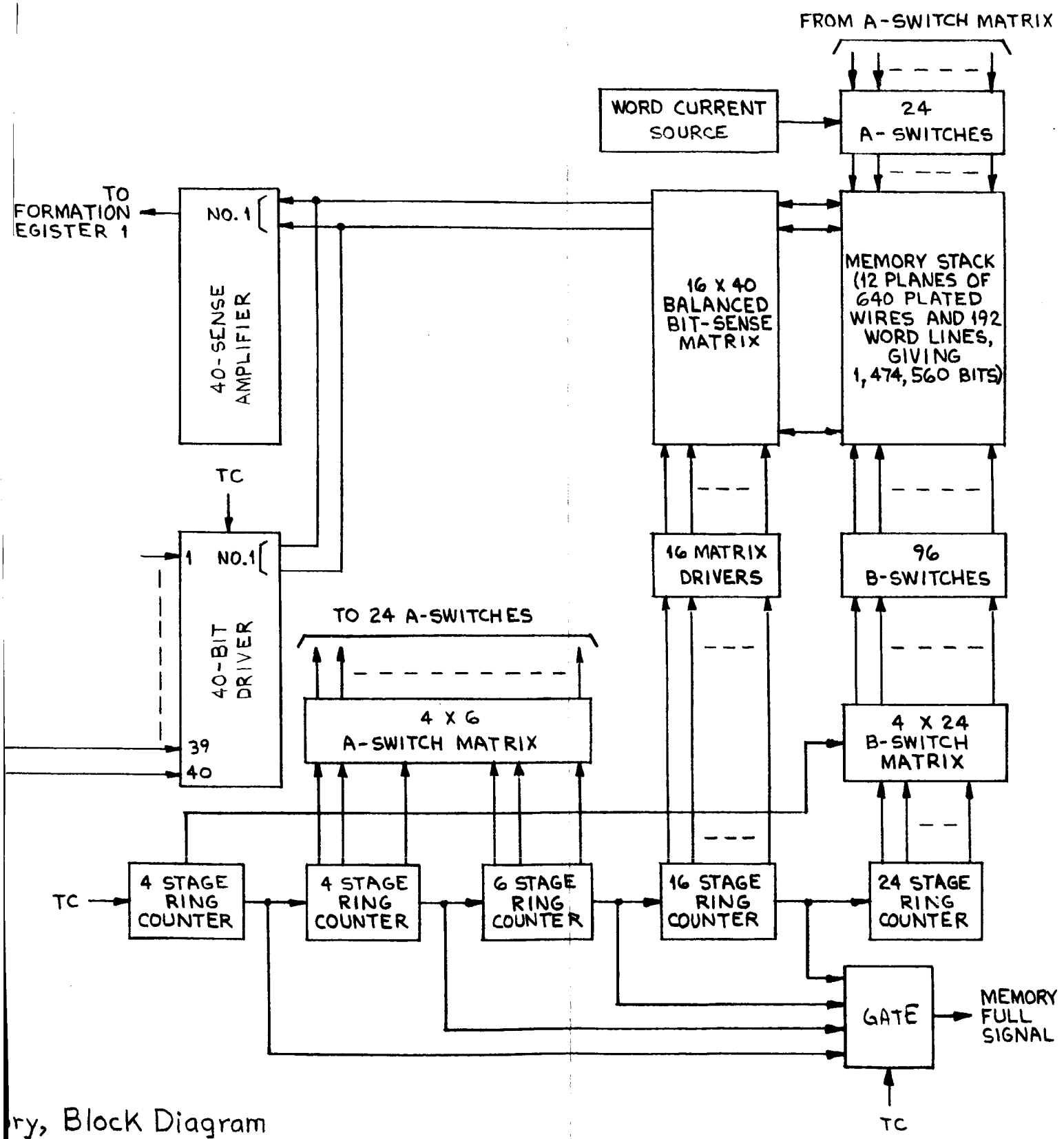


Figure 2-1. 1.4-Million Bit Mem



ry, Block Diagram

stored data may be read as many times as desired without regeneration or rewriting. Under these conditions the address counters cycle sequentially through all memory addresses and then repeat the cycle.

New data will be written into the memory at the first clock pulse following the change in command status from read to write. A total of 40 bits is temporarily accumulated in the low-power flip-flop information register, and then the 40 bits are simultaneously written into a position on 40 plated wires. Should the command status change from write to read when this register (see Figure 2-1) is partially full, the data will be lost (a maximum of 39 bits). A timing diagram for the write operation is shown in Figure 2-2. When the address counters reach the last address, a memory-full signal is provided.

Data will be read from the memory at the first valid clock pulse and each succeeding clock pulse after the write command changes to read. To provide the time necessary to reset all the address counters and read out the first 40 bits into temporary storage in the flip-flop information register, a 100-microsecond interval following the read command is provided. The memory timing circuits block the clock pulse from the memory during this period, and the clock pulses are ignored or invalidated. A timing diagram for the read operation is shown in Figure 2-3.

2.2. ORGANIZATION FOR MINIMUM POWER

The requirement that the memory be easily adapted for four-bit-parallel or one-bit-serial information requires the four-stage buffer register. During one-bit-serial data handling the four-stage buffer counter sequentially gates the data into the four-stage buffer register. The process is reversed for readout. That is, the four bits read into the buffer register are sequentially gated out one at a time onto the data output line.

At this point in the block diagram, Figure 2-1, the four-stage buffer register fills a 40-stage information register in 10 steps. The sequence of these steps is controlled by the ten-stage information counter. The size of this register, 40 bits, was determined in the following way: Equations were written for total memory power considering both standby and operating power of all the circuits. The predominant factor in these considerations was the balancing of the standby power of the 40 sense amplifiers and information registers against the pulse power required to energize the memory plane word readout drive line. Each word drive line pulse generates, nondestructively, signals in 640 plated-wire storage locations. For a fixed maximum information rate, 500,000 bits per second. This pulse power is inversely proportional to the number of bits processed in parallel. Pulse power (operating power) for the word driver is

$$P_{write} = \frac{P_{peak}\ (duration)}{2\ \mu s \times N} = \frac{0.8\ amp \times 24v \times 0.6\ \mu s \times 1.07}{2\ \mu s \times 40} = 0.153$$

where P_{peak} is the total instantaneous peak power drawn from the power supply and its capacitors.

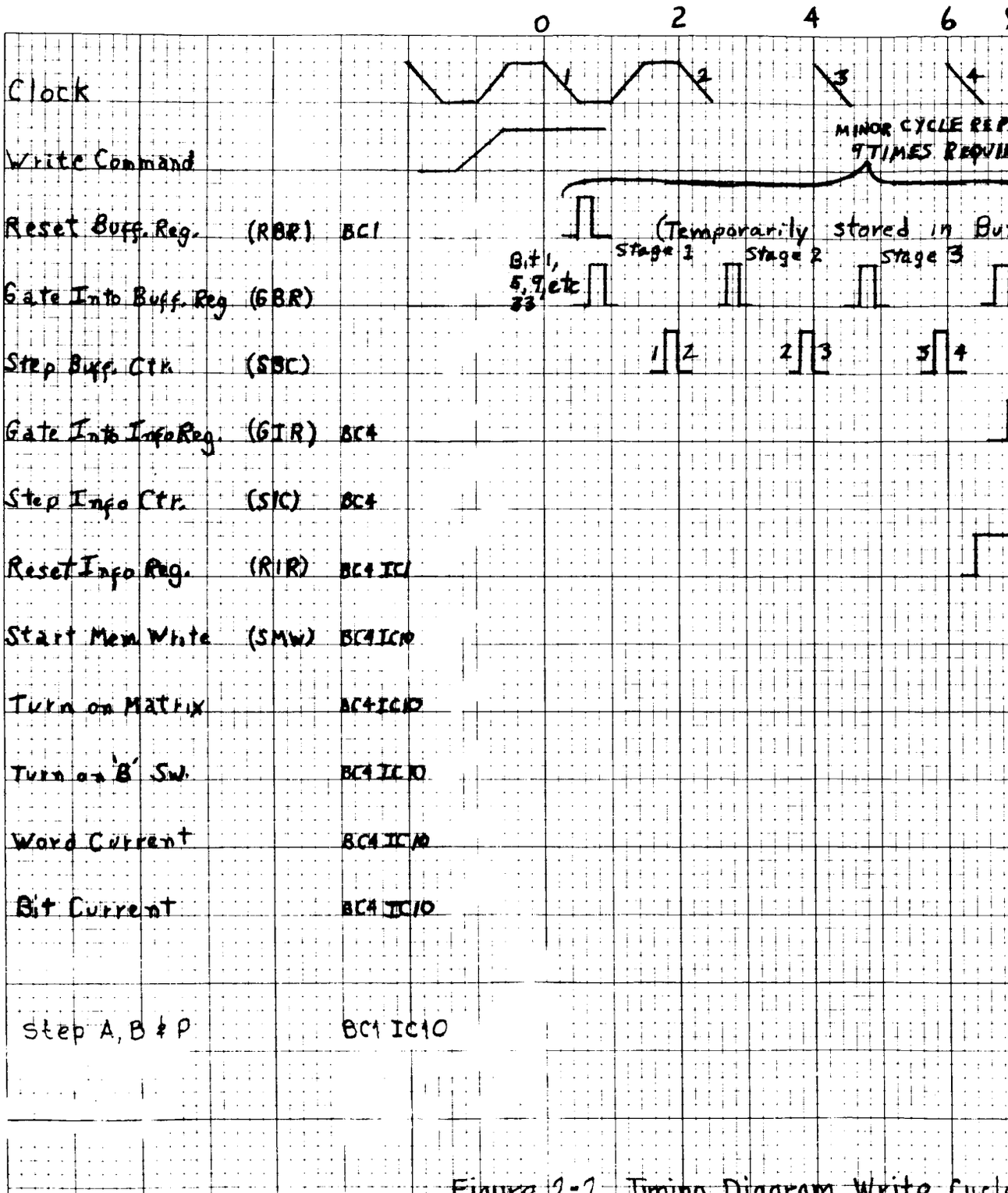
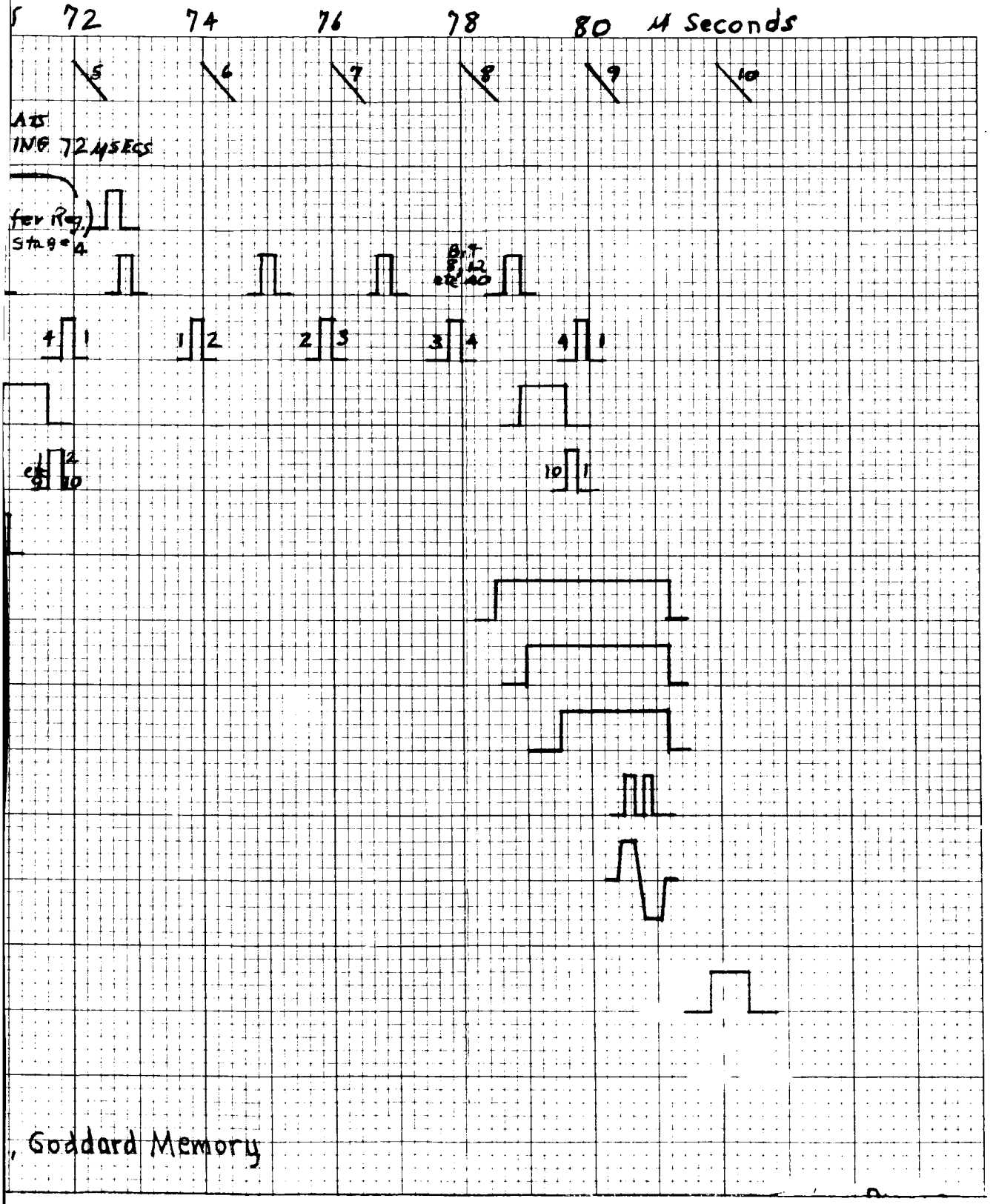


Figure 2-2. Timing Diagram Write Cycle

2


72
74
76
78
80
μ Seconds
5
6
7
8
9
10
ATS
ING 72 μSECS
fer Req.
Stage 4
4 1
1 2
2 3
3 4
4 1
10 1
, Goddard Memory

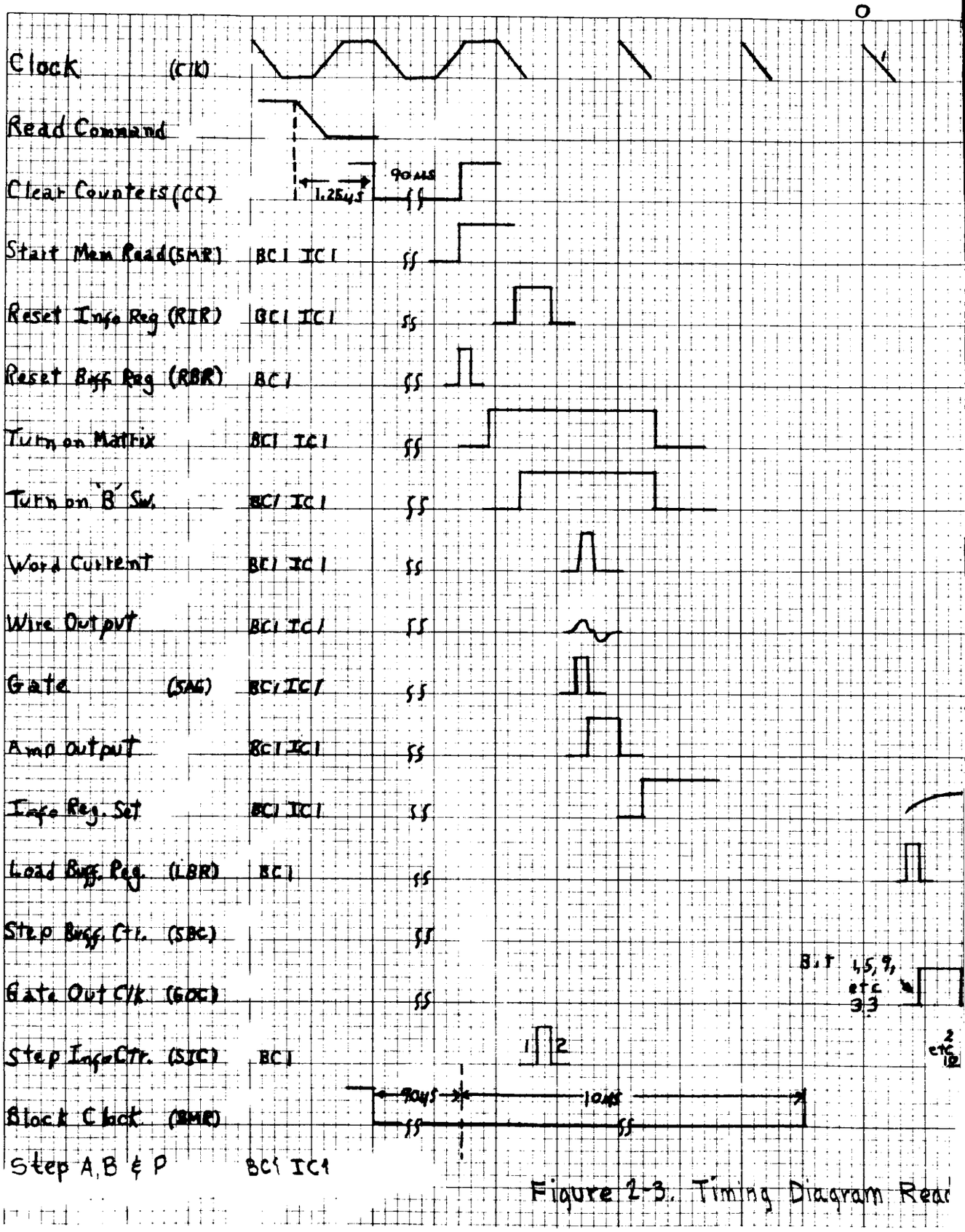
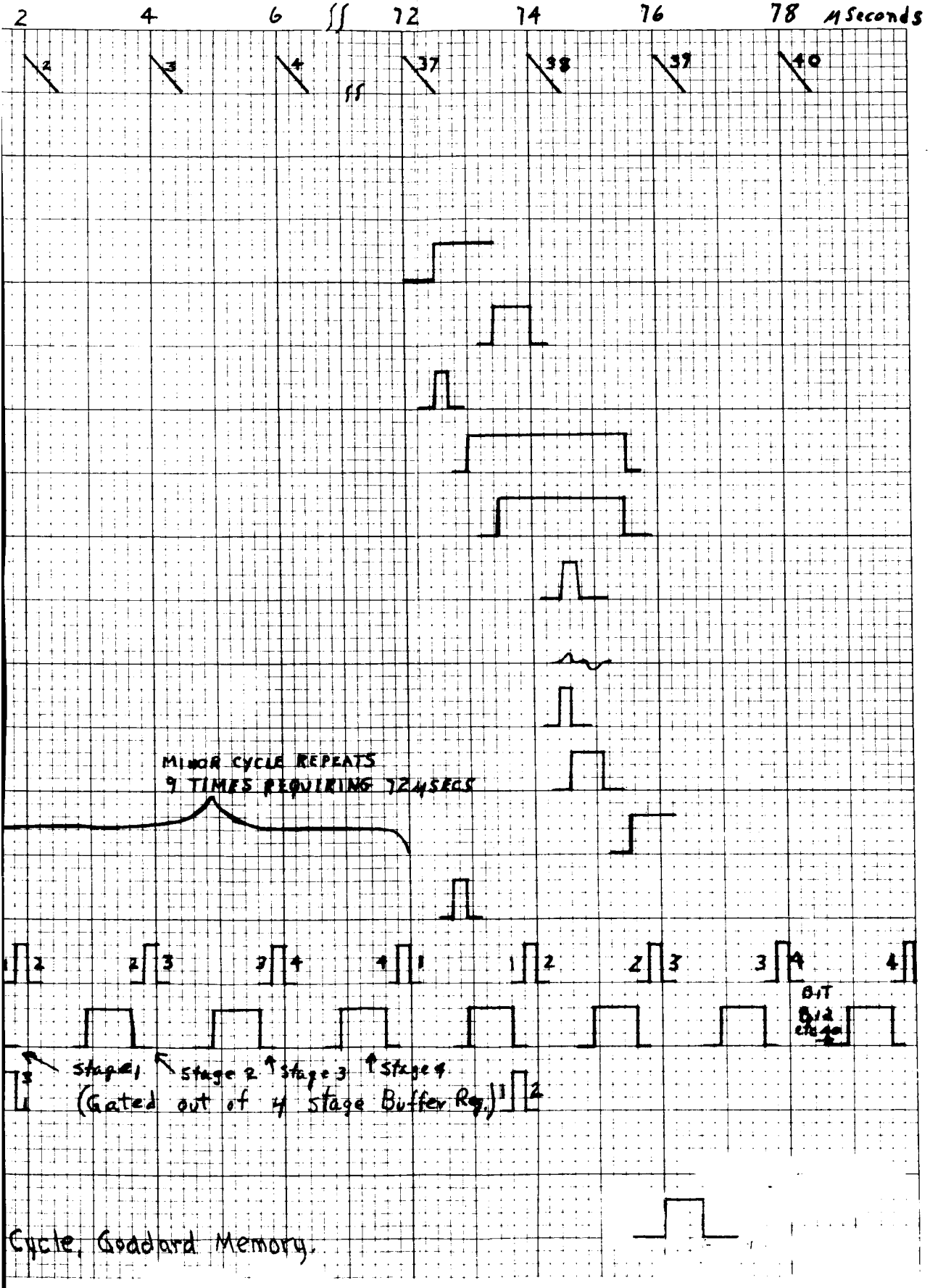


Figure 2-3. Timing Diagram Read



Cycle, Goddard Memory.

N = 40 = number of bits processed in parallel.

2 microseconds per bit is the maximum bit rate.

0.6 microsecond is the duration of the two word pulses to write.

1.07 is the efficiency factor.

For the bit driver

$$P_{write} = \frac{N\ (P_{peak})(duration)}{2\ N\ \mu s} = \frac{0.055\ amp\ x\ 12v\ x\ 0.7\ \mu s}{2\ \mu s} = 0.231$$

For the low level switch matrix

$$P_{write} = \frac{N\ (P_{peak})(duration)}{2\ \mu s\ x\ N} = \frac{0.006\ amp\ x\ 12v\ x\ 1\ \mu s}{2\ \mu s} = 0.036$$

The timing circuits pulse power is given by

$$P_{write} = \frac{(15\ circuits)(80\ mw)(0.75\ \mu s)}{N\ x\ 2\ \mu s} \times \frac{4}{3}\ efficiency$$

$$= \frac{1200\ mw\text{-}\mu s}{2\ N\ \mu s} = 15\ mw.$$

P_{write} total = 0.435

The standby power for the following circuits is given as follows:

Information register 1.5 mw x N	= 60 mw
Buffer register 11 mw	= 11 mw
Buffer counter 15 mw	= 15 mw
Sense amplifiers 5 mw x N	= 200 mw
A, B, and P counters 8 mw x 5	= 40 mw
Information counter 15 mw	= 15 mw
Timing circuits 5 mw x 10	= 50 mw
$P_{standby}$	= 391 mw

$P_{operating} = P_{standby} + P_{write} = 0.826$

A graph of these results for different values of N is shown in Figure 2-4.

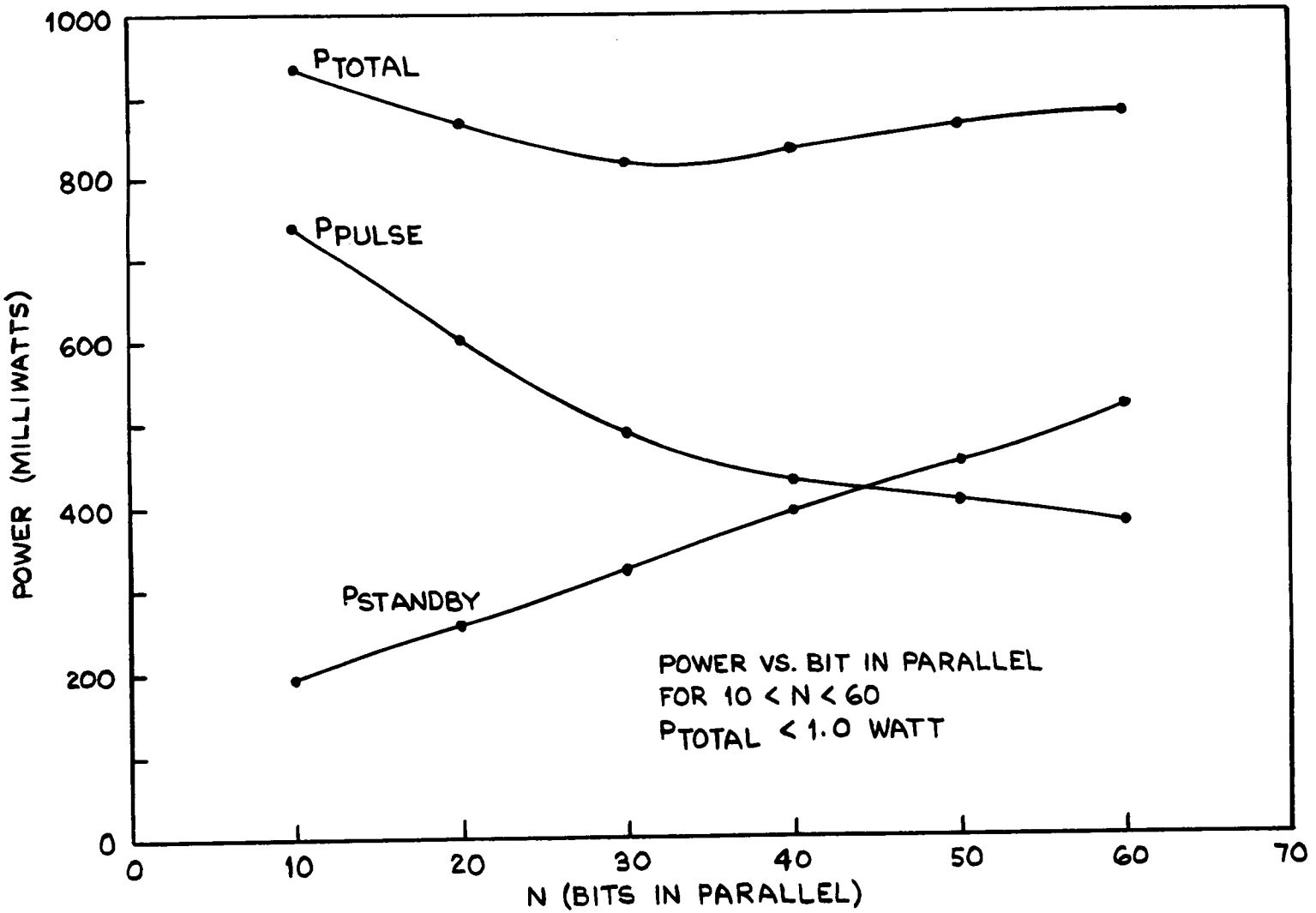


Figure 2-4. Power Consumption vs. Number of Bits Processed in Parallel

2.3. TIMING AND CONTROL FUNCTIONS

The timing and control circuits consist of a group of delay flops, flip-flops, gates, and driver circuits to generate all of the pulses to coordinate the many internal memory functions. The principal pulses required are as follows:

1. A standardized pulse for every valid clock pulse to step the four-stage buffer counter.

2. A standardized pulse for every valid clock pulse to time-gate the NRZ data into the four-stage buffer register.

3. A standardized pulse for every fourth valid clock pulse to step the ten-stage information counter.

4. A standardized pulse for every fourth valid clock pulse to time-gate information into and out of the ten-stage information register.

5. Two pulses every fortieth valid clock pulse when a write command is present to control the width and timing of the bit current relative to the word drive current.

6. A pulse every fortieth valid clock pulse when a read command is present to control the width and timing of a gate that puts the 40 sense amplifiers in a high gain state.

7. A pulse every fortieth valid clock pulse to step the 16-stage P counter.

8. A pulse every fortieth valid clock pulse to control the duration and timing of the drivers that turn on 40 out of 680 low-level switches connected to plated-wire storage elements.

9. Three pulses every fortieth valid clock pulse to control the duration and relative timing of the "on" period of 1 of 96 B switches, 1 of 24 A switches, and the word current pulse regulator.

2.4. RELIABILITY CALCULATIONS

A preliminary failure rate analysis has been made for the memory system design. This first analysis made the simplifying assumption that any component or joint failure caused the whole system to fail. This is, of course, a false assumption. An additional analysis will be made considering the partial system failure modes. For example, the failure of one word drive line diode would cause 640 successive bits to be indicated as 0's. This represents a loss of only 0.04 percent of storage capacity.

2.5. SUMMARY

The reliability evaluation is based on the product rule and exponential formula of reliability prediction.

$$P_s = e^{-t\lambda 1} \times e^{-t\lambda 2} \times e^{-t\lambda 3} \times \ldots\ldots \times e^{-t\lambda n}$$

$$P_s = e^{-t\ (\lambda_1 + \lambda_2 + \lambda_n)} = e^{-t\lambda t}$$

$$P_s = e^{-t\lambda t}$$

P_s = Probability of survival

t = A specified period of failure-free operation

m = Mean-time-between-failures

d = failure rate (The reciprocal of m)

The MTBF is calculated from:

MTBF = 10^5

MTBF = Mean time between failures in hours

= Failure rate in percent per 1000 hours

10^5 = Factor for converting percent per 1000 hours to hours

Reliability prediction based on the lowest obtainable failure rates. In most instances these failure rates were established to high reliability programs such as "Minuteman" specifications.

Solder joints - 15 billion joint hours without a failure - (Minuteman)

Failure rate = 45.79×10^{-6} failures per hour

MTBF = 21800 hours

P_s (Probability of success for one year, no failures of any kind)

$$= e^{-t/m} = e^{-\frac{8760}{21830}}$$

$$= e^{-0.401}$$

= 67 percent

Part or Assembly Description	Modules or Component Quantity	Mfg's. F.R.ea. c/o/1000 Hours	Applied Stress	Predicted F.R. With Derating	Module Failures Per Hour x 10^{-6}	Total Failures Per Hour
P-HC-02						
Bit Driver	40					
Resistors (Film)	6	0.001	10%	0.0005	0.030	
2N2501	2	0.001	50%	0.0007	0.014	
1N3207	10	0.00028	50%	0.00028	0.028	
				TOTALS:	0.072	2.880×10^{-6}
P-HC-03						
Matrix	140					
Resistors (Film)	8	0.001	10%	0.0005	0.040	
2N2501	4	0.001	50%	0.0007	0.028	
RT-184	4	0.001	50%	0.0007	0.028	
				TOTALS:	0.096	13.44×10^{-6}
P-HC-04						
Flip-Flop	40					
Resistors (Film)	9	0.001	10%	0.0005	0.045	
Capacitors	1	0.001	50%	0.005	0.005	
2N2501	2	0.001	50%	0.0007	0.014	
1N3207	14	0.00028	50%	0.00028	0.039	
				TOTALS	0.103	4.120×10^{-6}

Part or Assembly Description	Modules or Component Quantity	Mfg's. F.R. ea. c/o/1000 Hours	Applied Stress	Predicted F.R. With Derating	Module Failures Per Hour x 10^{-6}	Total Failures Per Hour
P-HC-05						
Counter	84					
Resistors (Film)	10	0.001	10%	0.0005	0.050	
Capacitors	1	0.001	50%	0.0005	0.005	
2N2501	2	0.001	50%	0.0007	0.014	
2N3251	1	0.001	50%	0.0007	0.007	
				TOTALS:	0.076	6.384×10^{-6}
Switch Drivers	15					
Resistors	3	0.00067	10%	0.0003	0.009	
2N2501	2	0.001	50%	0.0007	0.014	
1N3207	2	0.00028	50%	0.00028	0.0056	
				TOTALS:	0.0286	0.1430×10^{-6}
Additional Components						
Resistors	300	0.0067	10%	0.0003	0.900	
Capacitors	10	0.001	50%	0.0005	0.050	
Transistors	100	0.001	50%	0.0007	0.700	
1N3207	300	0.00028	50%	0.00028	0.840	
				TOTALS:	2.490	2.490×10^{-6}

Part or Assembly Description	Modules or Component Quantity	Mfg's. F.R. ea. c/o/1000 Hours	Applied Stress	Predicted F.R. With Derating	Module Failures Per Hour x 10^{-6}	Total Failures Per Hour
Word Line Diode						
1N3207	2200	0.00028	50%	0.00028		6.16×10^{-6}
P-HC-06						
Read Amplifier	40					
Resistors (Film)	15	0.001	10%	0.0005	0.075	
Capacitors	6	0.001	50%	0.0005	0.030	
2N2501	1	0.001	50%	0.0007	0.007	
2N3251	2	0.001	50%	0.0007	0.014	
2N3493	3	0.001	50%	0.0007	0.021	
1N3207	1	0.00028	50%	0.00028	0.0028	
				TOTALS:	0.1498	5.992×10^{-6}
P-HC-07						
A-Switch	48					
Resistors (Film)	3	0.001	10%	0.0005	0.015	
2N2501	2	0.001	50%	0.0007	0.014	
1N3207	1	0.00028	50%	0.00028	0.0028	
				TOTALS:	0.0318	1.5264×10^{-6}

Part or Assembly Description	Modules or Component Quantity	Mfg's. F.R. ea. c/o/1000 Hours	Applied Stress	Predicted F.R. With Derating	Module Failures Per Hour x 10^{-6}	Total Failures Per Hour
P-Drivers	18					
Resistors (Discrete)	3	0.0067	10%	0.0003	0.009	
2N2501	1	0.001	50%	0.0007	0.007	
1N3207	2	0.00028	50%	0.00028	0.0056	
				TOTALS:	0.0216	0.3888×10^{-6}
B-Switches	88					
Resistors	3	0.00067	10%	0.0003	0.009	
2N2501	2	0.001	50%	0.0007	0.014	
1N3207	1	0.00028	50%	0.00028	0.0028	
				TOTALS:	0.0258	2.2704×10^{-6}

SECTION 3

MEMORY CIRCUIT DESIGNS

This section of the interim engineering report briefly describes all the circuits designed for the 1.4×10^6-bit Miniature Spaceborne Memory. Appendix I to this report provides a detailed description of each circuit's operations, the design equations, and test results. A composite components list (Appendix II) tabulates the manufacturer and the maximum stress to which each component is subjected.

3.1. LOGIC AND CONTROL CIRCUITS

These circuits compose the interface with external equipment, generate all necessary timing pulses, and control the address counters. These circuits include the following:

1. A monostable multivibrator that generates control pulses and uses no standby power.

2. An information buffer register that changes bit serial information to 4 bit parallel during a write cycle and reverses the operation during a read cycle.

3. A low-power ring counter that controls and synchronizes the buffer register operation.

4. A number of special-purpose circuits such as the counter inverter and amplifier, the counter pulser, a pulse amplifier, a pulse gate, a counter stepping circuit and buffer register reset, an output buffer, a logic inverter and amplifier, a logic gate, a low-power information register, and an output flip-flop.

3.2. INFORMATION PATH CIRCUITS

These memory circuits receive low-level signals directly from the memory elements (bit-sense switch matrix and sense amplifier) and convert them to a standardized digital pulse format. They also accept standardized digital pulse information to be stored (the bit driver) and change it into currents which cause the memory elements to store the information. In addition, circuits closely related to the operation of the circuits mentioned above are described.

3.2.1. READ AMPLIFIER

The function of the read amplifier is to amplify and detect the plated wire information output signal, while repeating unwanted common-mode signals, and to provide an output signal that indicates whether a 1 or 0 has been detected. The output of the amplifier provides a pulse to the information register if a 1 is detected and no pulse if a 0 is detected. The amplifier is gated during the period of time that the plated wire information output signal is present at the amplifier input. The only 0 signal required is that necessary to overcome transient noise; therefore the 1 signal requirement is the one which must be met.

A minimum 1 signal of 93 millivolt-nanoseconds is required at the input of the circuit to give the output pulse. The circuit has a minimum common-mode rejection of 28 and requires 3.33 milliwatts of steady-state power.

The circuit is built using screened ceramic resistors. Capacitors have been eliminated in the design of the amplifier wherever possible to make the hybrid circuitry as simple as possible.

Forty sense amplifiers are used to process forty bits of information in parallel.

3.2.2. BIT-SENSE SWITCH MATRIX

The bit-sense switch matrix selects the plated wire from which information is to be read during a read cycle or into which information is to be written during a write cycle. The bit-sense switch matrix is comprised of a group of transistor switches which provide a low impedance between the selected plated wire in a bit group and the read amplifier and bit driver. Transient voltages not related to the stored information are rejected by using a dummy balancing wire connected to one side of the differential amplifier. Transient noise coupling through the capacitance of the switches which are off is cancelled by using a balanced bit-sense matrix. An equal number of switches are connected to each side of the differential amplifier, which is the first stage of the read amplifier.

This switch matrix connects each sense amplifier (bit driver during a write command) to one of a group of 16 plated wires and one of two dummy wires. Forty amplifiers (and/or bit drivers) require 720 switches in the matrix.

3.2.3. BIT DRIVER

The function of the bit driver is to drive pulses of current down the plated wire during the memory write cycle, in time coincidence with the word current. This writes new information in the plated wire. The bit driver supplies two sequential pulses of current of opposite polarity to represent a 1 and a 0. The time at which the pulses occur in the memory cycle is controlled by two timing pulses. Two logic inputs from the information register determine whether a 1 or a 0 is to be written.

The bit drivers require 215 milliwatts of pulse-power operating at a 2-microsecond serial bit rate. Forty bit drivers are used to process forty bits of information in parallel.

3.2.4. MATRIX DRIVERS

The matrix driver supplies equal positive and negative-going pulses which select the matrix switches that are turned on in the memory cycle. The matrix driver is designed to drive 40 matrix switches in parallel, since 40-bit-parallel operation is used when reading from or writing into the memory stack. The output pulses must swing to 6 volts minimum with respect to ground and must be capable of supplying 2.81 milliamperes per load, or a total of 112 milliamperes. The required input current from the counter which selects the matrix position is 22.7 milliamperes.

Eighteen matrix drivers are used in the memory system. Matrix drivers numbered 1 through 8 (used one at a time) cause the switch matrix to connect the corresponding plated wire to the first terminal of the sense amplifier input, while matrix driver number 17 causes the switch matrix to connect a dummy wire to the second input to the differential amplifier. Matrix drivers 9 through 16 (used one at a time) cause the corresponding wire to be connected to the second input terminal, while matrix driver 18 causes the other dummy wire to be connected to the first terminal of the differential amplifier.

3.2.5. BIT PATH INTERFACE CIRCUITS

The three bit path interface circuits are the bit power pulser, the bit timing pulser, and the read gate pulser; these three circuits are driven by delay flops which provide the pulse timing.

The bit power pulser provides the voltage pulse which steps up the current level of the information registers. The output must swing from ground to 11.1 volt minimum and must be capable of supplying a total of 84 milliamperes (2.1 millamperes to each of 40 information registers).

The bit timing pulser provides the voltage pulse which activates the bit drivers. The output must swing from -3 volt to 11.1 volt minimum and be capable of supplying a total of 520 milliamperes (13 millamperes to each of 40 bit drivers).

The read gate pulser provides the voltage pulse to drive the read amplifier gates. The output must swing from ground to 5.4 volt minimum and be capable of supplying 1.45 milliamperes to each gate. The output must also be capable of driving 31 picofarads per gate.

3.3. WORD LINE DRIVE, SELECTION, AND COUNTER CIRCUITS

These circuits generate a regulated amplitude current pulse which is steered to a selected word line to read out or write information in the plated wire memory element. The counter circuits generate the sequential addressing of all storage locations in the memory.

3.3.1. WORD CURRENT SOURCE

The word current source is a current regulator circuit which must drive a closely controlled pulse of current of 800 milliamperes through a word line. The pulse should have a rise time of 100 to 150 nanoseconds, a fall time of 30 to 40 nanoseconds, and a flat top lasting about 100 to 200 nanoseconds as controlled by the input. Information stored in the wire is sensed on the trailing edge, which permits a slow leading edge and eliminates overshoot and ringing. The word current source is designed to minimize pulse width variation, since instantaneous peak power dissipation in the system is high when word current flows. Only one word current source is used in each 1.4×10^6-bit half-memory.

3.3.2. WORD CURRENT SWITCHES AND SWITCH DRIVERS

The word current switches and switch drivers select 1 of 2304 word lines in the 1,400,000-bit half-memory by means of a two-dimensional diode matrix. The two coordinates, A and B, of the matrix are selected through switches. The system comprises 24 A-switches and 96 B-switches. A significant saving in hardware is effected by the use of a 4 x 6 matrix selection of the A-switch and a 4 x 24 matrix selection of the B-switch.

To drive word current down the line, the proper A-switch and B-switch are driven by the respective drivers; then the word current source is pulsed. To terminate the word current, this sequence is reversed.

3.3.3. LOW POWER RING COUNTER

The ring counter, which is used for address selection, uses complimentary transistors. It dissipates a maximum of 6.3 milliwatts in the standby mode, regardless of the number of stages, and can drive heavy loads by augmenting its input current momentarily. The counter can be stepped every microseconds or slower. The circuit can be designed by use of low-tolerance components, both passive and active, and thus lends itself to thin-film and hybrid circuit manufacture.

Four ring counters, two with four stages, one with six stages and one with 24 stages are associated with the word line-addressing and selection function.

3.3.4. RING COUNTER AUXILIARY CIRCUITS

The low-power ring counters require four auxiliary circuits for their operation; these are the stepper, high level driver, reset, and level shifter circuits. The first three circuits are required for operating a single ring counter, while the level shifter circuit is used when one ring counter is to be stepped whenever a second counter reaches a predetermined count. This action would occur when the two counters form a two-dimensional matrix so that an M-stage counter and an N-stage counter drive (M x N) leads.

SECTION 4

THE PLATED-WIRE MEMORY ELEMENT

The memory element consists of a wire substrate which is made of beryllium-copper drawn to a 0.005-inch diameter and which is electroplated with a magnetic thin film. The magnetic film is the same 81 percent nickel, 19 percent iron alloy widely used in planar thin-film memory elements. The coating is continuous and is plated in the presence of a circumferential magnetic field that establishes a magnetic anisotropy axis, or preferred magnetization direction, circumferentially around the wire. Figure 4-1 is a simplified diagram of the plating apparatus and the electrical test that provides immediate control of the process. The magnetic material is electroplated on a continuously moving wire in room environment. The continuously moving wire is electrically tested with a complete operating memory pulse program.

Information is stored according to the sense of the circumferential magnetization in the portion of the plated wire encircled by the word strap: clockwise magnetization represents a stored 1; counterclockwise magnetization represents a stored 0. Figure 4-2 shows a sketch of the plated wire and the word drive line which forms a one-turn solenoid encircling many plated wires (only one is shown). To read the stored information, a word current is applied to the word strap which encircles the plated wire at right angles. The word current produces a word field along the axis of the wire. This word field tilts the magnetization vector from its circumferential rest position towards the axis of the wire. The resulting flux change causes a voltage change (sensed at the ends of the plated wire) of one polarity for a stored 1, and of the opposite polarity for a stored 0. Figure 4-3 shows a qualitative vector diagram of the magnetization vector position. The amplitude of the word current is controlled so that when the current is turned off the magnetization vector returns to its original rest position under the influence of the anisotropy and demagnetizing fields; thus, the readout is nondestructive.

Information is written into the wire by the time coincidence of the word current and a steering bit current through the plated wire. When the bit current flows in one direction, the magnetization vector is so steered that when the bit and word current end the vector is in the 1 rest position; when the bit current flows in the other direction, the magnetization vector is left in the 0 position.

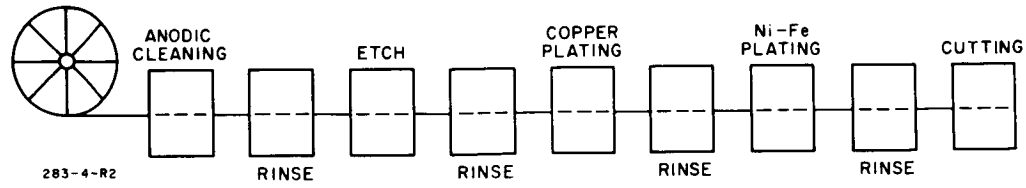


Figure 4-1. Wire Plater and Tester

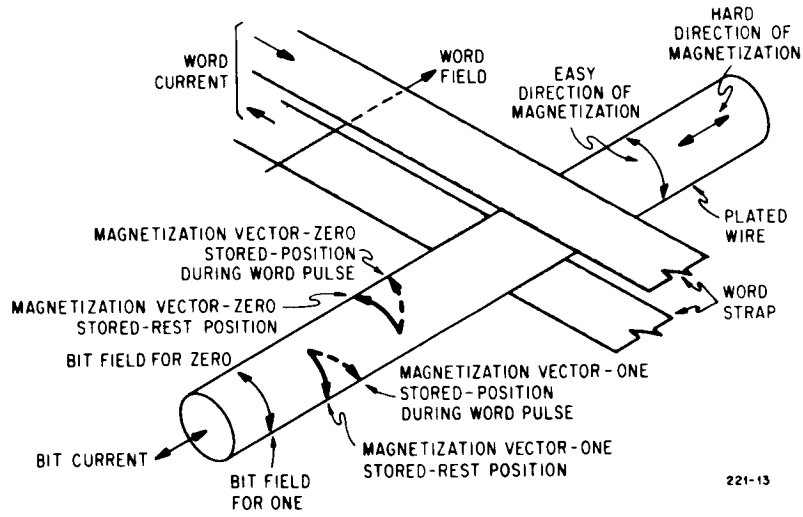


Figure 4-2. Information Storage on Plated Wire

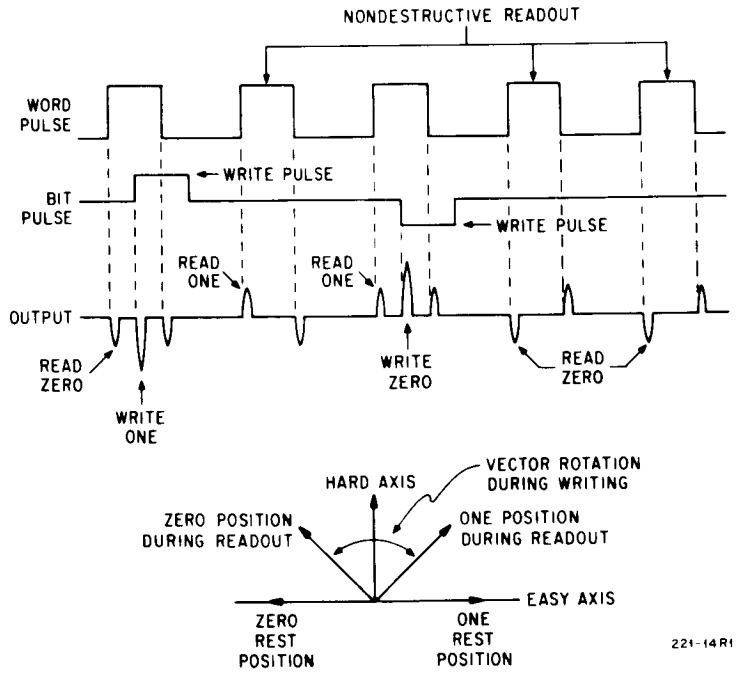


Figure 4-3. Read and Write Operations

Operating parameters of the plated wire for the Miniature Spaceborne Memory are as follows:

Word-strap width:	33 mils, 1/2 turn,
Word current:	800 milliamperes
Bit current:	35 milliamperes
Output voltage:	±10 millivolts nominal, 5 millivolts worst-case with off-nominal currents
Switching time:	80 nanoseconds (for a 40-nanosecond fall time word current)

It is important to note that the same amplitude word drive current used for reading is also used for writing. The word drive current in the drive line must not adversely affect the information stored in the nonselected words. Similarly, the bit write current that flows in the plated wires must control the magnetization direction in only the one selected bit.

The magnetic plating is continuous and if more than 20 to 25 bits per inch along the wire are used there is a tendency for them to interfere with each other. This interference is reversible. If 0 is written millions of times on each side of a 1 with the program shown in Figure 4-3 the signal read from the 1 will be diminished. If 1 is written on each side of the center test bit, the signal read from the test bit will be increased. This effect is nearly eliminated by the use of the writing technique shown in Figure 4-4. This method of writing, called phase modulated writing, depends upon the reversibility of the adjacent-bit interference. It eliminates this interference by always writing an equal number of 1's and 0's independent of the stored information. It also eliminates any magnetic history effect. Most magnetic storage elements exhibit a sensitivity to the polarity of the information stored in the preceding write operations. Phase modulated writing means that every storage location experiences equal numbers of 1's and 0's in the preceding write operations.

4.1. PLATED-WIRE TEST SPECIFICATION

A number of tests were performed to enable a detailed test specification to be written for the plated wire to be used in the Miniature Spaceborne Memory. The following is a list of the items investigated:

1. The effect of adjacent plated wires on operating parameters.
2. The variation of item 1 as a function of word strap width.
3. The variation of item 1 as a function of the type of adjacent wire.
4. The operating parameters of various word strap widths and word line configurations:
   a. Two-turn word line solenoids.
   b. One-turn word line solenoids.

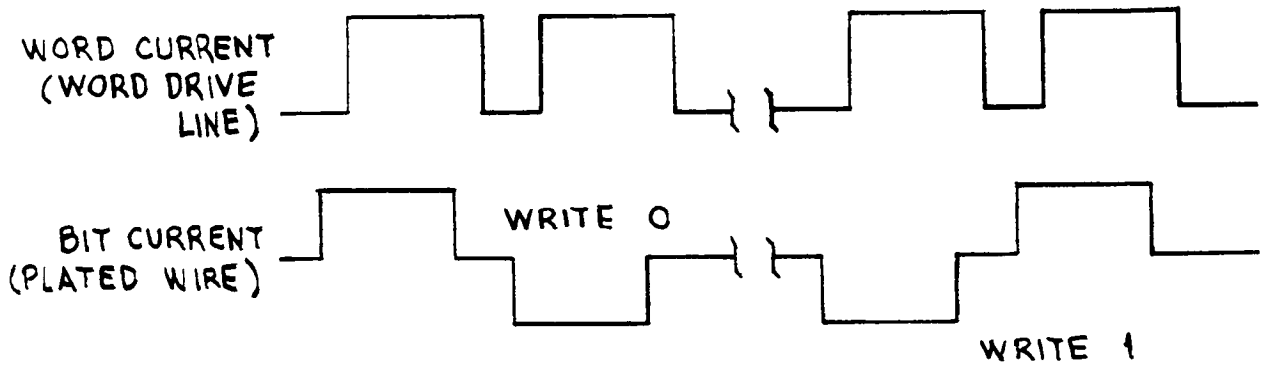


Figure 4-4. Phase Modulated Write

c. Half-turn word line with a copper ground plane return.

d. Half-turn word line with an aluminum ground plane return.

Each of the word line configurations was tested using both copper word straps and copper clad mu-metal word straps. The tests were conducted in two phases:

Phase I - Items 1 through 4 a using the two-turn word line solenoid for all tests.

Phase II - Items 4 b through 4 d.

4.1.1. PHASE I

Introduction

Two evaluation planes were prepared for testing. Both planes used 0.015 inch centers on the plated wires. One plane (EP_1) contained copper word lines 0.0013 inch thick. The other plane (EP_2) had word lines made of mu-metal 0.001 inch thick plated with 0.0008 inch of copper. Each plane had six sets of word lines with three word lines per set. Only three of these sets were used for the tests. Each word line consisted of two turns. The space between the two turns was 0.005 inch and the center to center spacing was 0.045 inch. The sets tested are as listed below:

Set Number	Guard Band (space between word lines)
4	0.018 inch
5	0.014 inch
6	0.010 inch

The plated wires used for the tests were wires that were in the "accept" category from another requirement.

To evaluate the items being investigated, data was taken on the following parameters:

Iw_p - Word current necessary to write

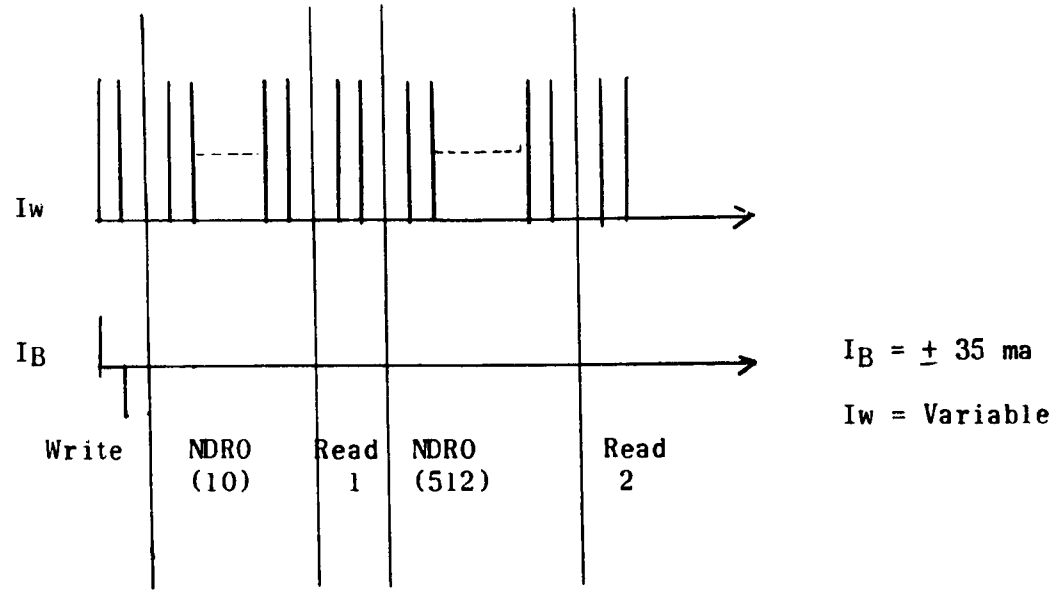
Iw_d - Word current necessary to destroy

Iw_a - Adjacent bit disturb word current

E_o - Single write disturbed output after an entire pulse program.

1. Iw_p and Iw_d:

The program used for Iw_p and Iw_d is shown in the following figure:



Numbers in parentheses indicate the number of times that function is performed per program.

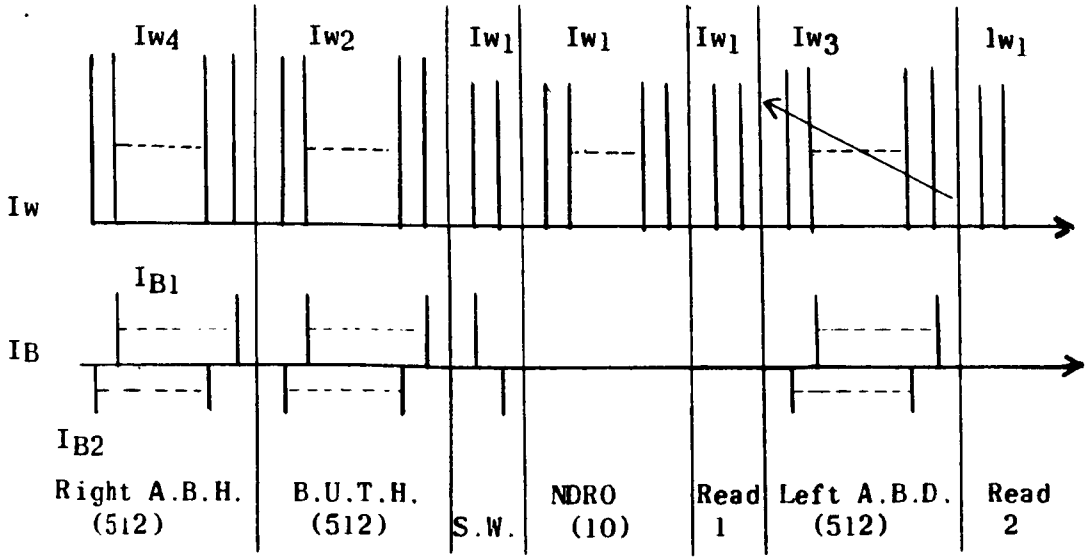
Program is repeated with opposite polarity bit currents.

Iw_p is found by observing the output voltage due to Read 1 while increasing Iw from a value much less than Iw_p until the bit under test just starts to write, then $Iw = Iw_p$.

Iw_d is found by comparing the output voltages due to Read 1 and Read 2 while increasing Iw. When the peak of the output voltages begin to separate, then $Iw = Iw_d$.

2. Iw_a:

The program used to determine Iw_a is shown below.



A.B.H. - Adjacent bit history.
B.U.T.H. - Bit under test history.
S.W. - Single write.
A.B.D. - Adjacent bit disturb.

Numbers in parentheses indicate the number of times that function is performed per program.

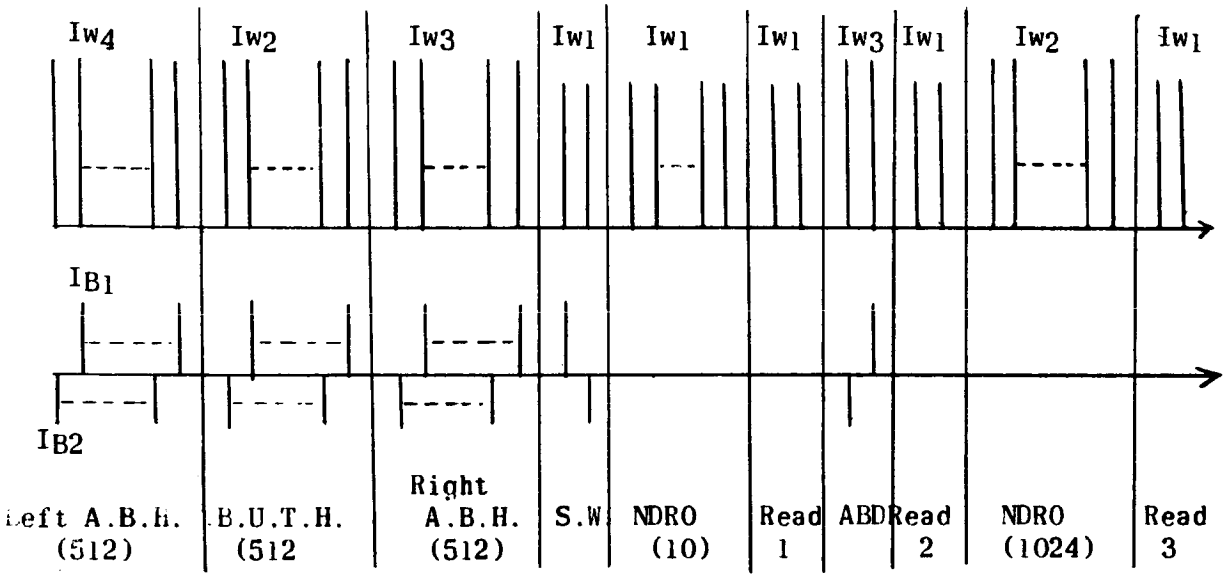
Program is repeated with opposite polarity bit current.

Current Amplitudes: I_{w2}, I_{w4} = 1.05 Iw (nom.)
I_{w1} = 0.95 Iw (nom.)
I_{w3} = variable
I_{B1} = 37 ma
I_{B2} = 33 ma

The method used to find I_{w_a} is as follows: Observe the output voltages due to Read 1 (E_{o1}) and Read 2 (E_{o2}). Increase I_{w3} until $E_{o2} = 0.75\ E_{o1}$. Then $I_{w3} = I_{w_a}$.

3. E_{out}:

The program used to find the single write disturbed output voltage is shown below. Only one adjacent bit disturb is used since the Miniature Spaceborne Memory is a sequentially addressed buffer memory.



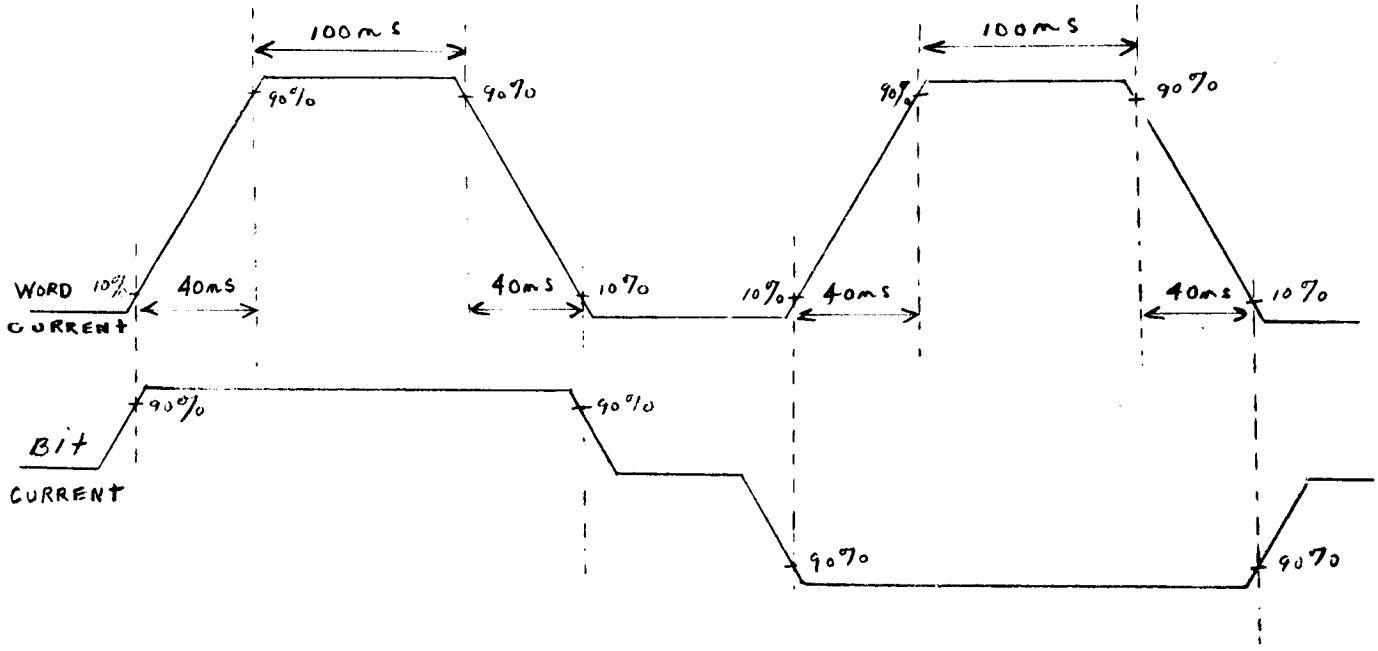
Numbers in parentheses indicate the number of times that function is performed per program.

Program is repeated for opposite bit current polarities.

Current Amplitudes: I_{w1} = 0.95 Iw (nom.)
$I_{w2} = I_{w3} = I_{w4}$ = 1.05 Iw (nom.)
I_{B1} = 37 ma
I_{B2} = 33 ma

The output voltages were recorded at Read 1, 2 and 3.

The current shapes and timing for all pulses were as shown below:



A rise time of 40 nanoseconds was used for all readout word currents.

Procedure

Plated wires were selected from a group that was of good quality and had low sensitivity to twist. Plane EP_1 was checked for noise with a copper wire. With a rise time equal to 40 nanoseconds, a current amplitude of 800 milliamperes, and using word line set number 4, the noise was 0.5 millivolt. Current amplitude variations were performed with decibel pads. These pads had a 0 to 11 decibel range variable in 0.1 decibel steps.

Part 1. Load plane EP_1 with test wire (T.W.).
Using word line set number 4:

a. Find I_{wp} and I_{wd}.

b. Load adjacent wire number 1 and repeat step a.

c. Load adjacent wire number 2 and repeat step a. Continue until I_{wp} and I_{wd} reach an asymptotic condition.

Repeat steps a, b, c, for word line set number 5 and set number 6.

Repeat steps a, b, c, for EP_2 word line set number 5.

Part 2. Using Plane EP_1 and the required number of fill wires as found in Part 1, perform the following test on five test wires:

a. Find Iw_p and Iw_d.

b. Calculate Iw (nom.) = 1.15 Iw_p (average).

c. Find adjacent bit disturb current.

d. Find E_{out}.

e. Repeat steps a through d for word lines set number 5 and set number 6.

Part 3. Repeat Part 2 on plane EP_2.

Part 4. To investigate further the effects of adjacent wires, perform the following test on Plane EP_2:

a. Find Iw_p and Iw_d on test wire number 1.

b. Remove adjacent wire and repeat step a.

c. Place "Kovar" wire in adjacent groove and repeat step a.

d. Replace "Kovar" wire with original plated wire.

e. Repeat steps a through d on test wires number 2 through number 5.

f. Change wires to Plane EP_1 and repeat steps a through e.

As a regular part of the test procedure, the testing system was calibrated every morning before beginning tests and every evening after completing tests to ensure no drifting of the equipment. Also, current amplitudes were checked before and after each test.

Results

Part 1. The effect of adjacent wires on Iw_p and Iw_d for the three sets of word lines on EP_1 is shown in Figure 4-5. These curves indicate the same basic changes occur for each size, for example, an increase of operating parameters

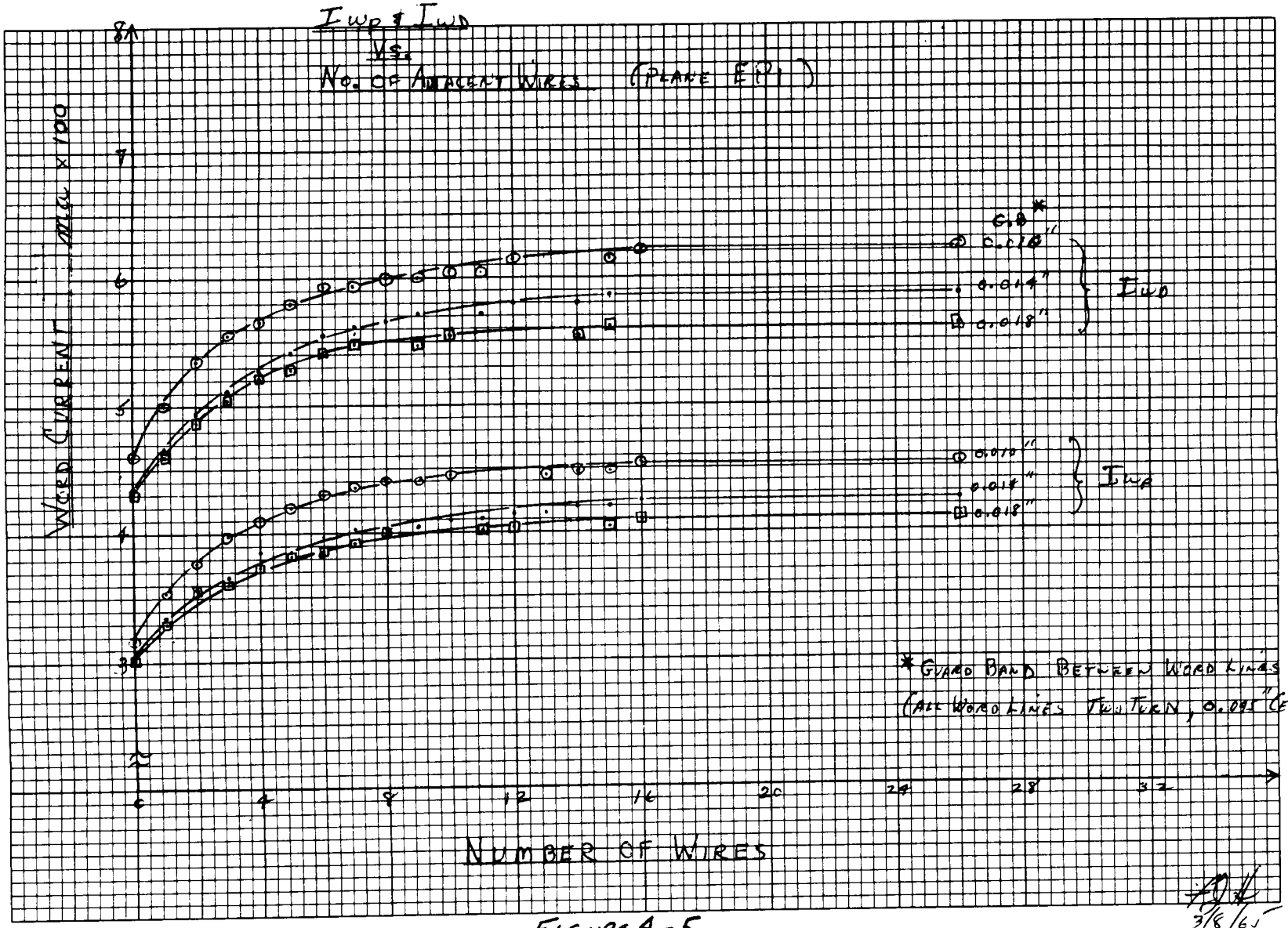

I_{WP} & I_{WD}
Vs.
No. of Adjacent Wires (Plane #1)
Word Current - ma x 100
8
7
6
5
4
3
2
1
0
4
8
12
16
20
24
28
32
Number of Wires
0.0
0.010"
0.014"
0.018"
I_{WD}
0.010"
0.014"
0.018"
I_{WP}
*Guard Band Between Word Lines
(All Word Lines Two Turn, 0.095" Centers)
3/6/63

FIGURE 4-5

with the addition of adjacent wires. The asymptotic values of I_{wp} and I_{wd} occurred at about the same number for each set - eight wires on both sides of the test wire. Table 4-1 tabulates the results.

Table 4-1

Word Line Set No.	Percent Change		Nominal Operating Current and Range (ma)		Percent Change in Nominal Current
	I_{wp}	I_{wd}	No Adjacent Wires	Asymptotic Condition	
4	+28.0	+32.8	366 ± 17.5%	486 ± 15.6%	+32.8
5	+25.4	+28.6	370 ± 17.6%	506 ± 16.0%	+36.8
6	+23.4	+28.6	379 ± 16.1%	538 ± 15.7%	+42.0

The following two things are evident from Table 4-1:

1. the operating range decreases with the addition of adjacent wires, and

2. the change in the nominal current increased the most for set number 6 (the widest word line width).

Figure 4-6 compares the results of the adjacent-wires test on EP_1 and EP_2 using word line set number 5. The results of EP_2 indicate an asymptotic condition at about the same number of wires as EP_1. The changes are slightly different and are summarized in Table 4-2.

Table 4-2

Plane	Percent Change		Nominal Operating Current and Range (ma)		Percent Change in Nominal Current
	I_{wp}	I_{wd}	No Adjacent Wires	Asymptotic Condition	
EP_1	+25.4	+28.6	370 ± 17.6%	506 ± 16.0%	36.8
EP_2	+39.0	+25.8	278 ± 16.5%	364 ± 11.5%	31.0

Table 4-2 and Figure 4-6 show that the changes which occur because of adjacent wires are not too different between EP_1 and EP_2. The only disagreement is in the change in I_{wp}. This, in turn, caused a big different in the operating ranges at the asymptotic condition.

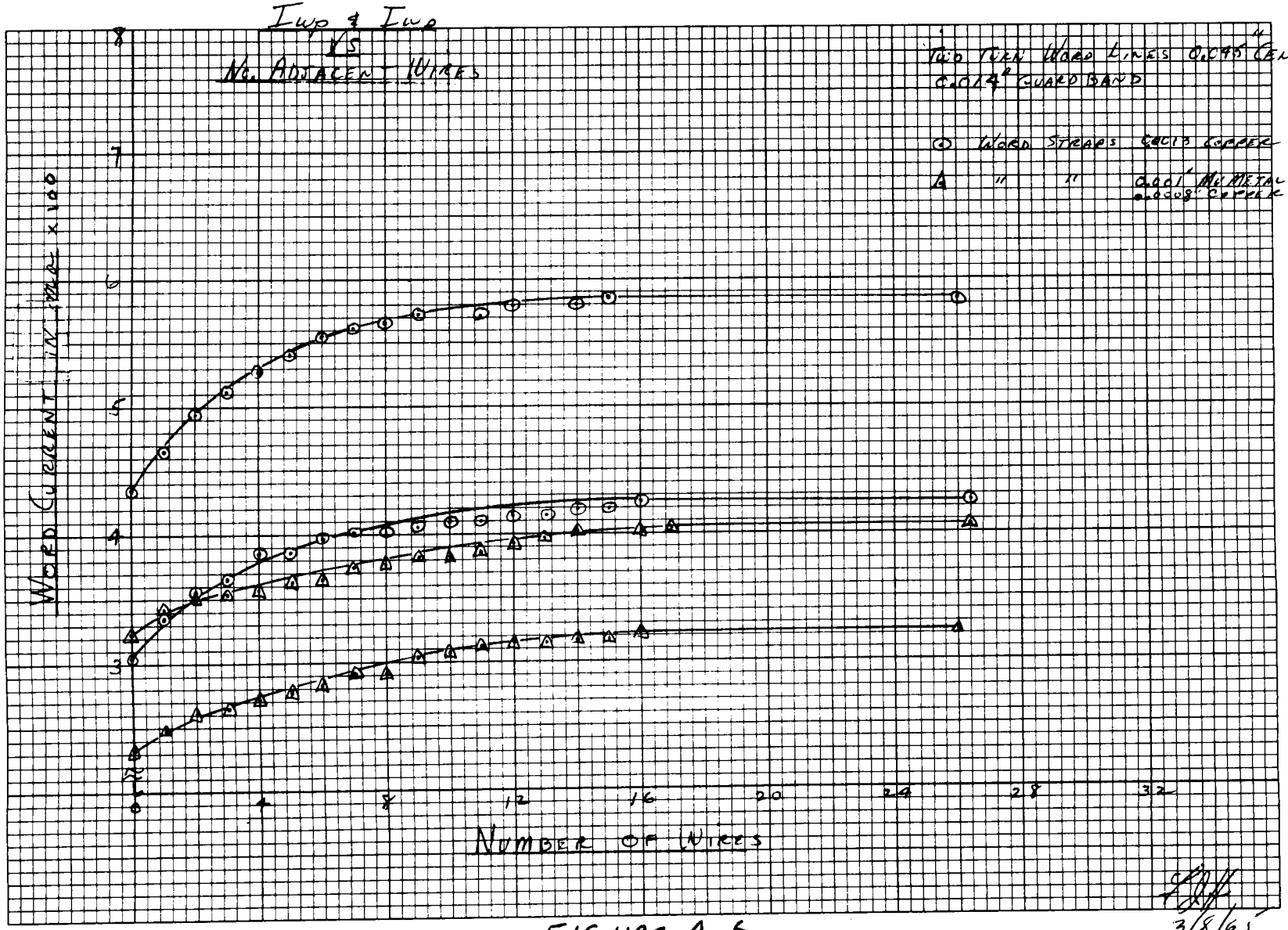


FIGURE 4-6

3/8/65

Part 2. The results of Part 2 are plotted in Figure 4-7. From the curves it can be seen that set number 6 had the best overall operating conditions. The output increased with increasing word strap width while the operating range was about the same for each word strap set. The operating range is defined as

$$\text{Iw (nominal)} \pm \frac{I_D}{\text{Iw (nom.)}} \times 100 \quad \text{percent}$$

where $\text{Iw (nominal)} = Iw_p + I_D$ and $I_D = \frac{Iw_d - Iw_p}{2}$.

An unexpected result was the fact that $Iw_a \simeq Iw_p$. Further investigation of the effects of adjacent bit current showed that three out of the five bits tested lost 50 percent or less of their peak output voltages when the current was increased to two and one-half times Iw_a. The other two bits lost between 75 and 100 percent. This effect was probably due to a lack of history on one side of the test bit.

The disturbed output voltage (E_{out}) in all cases was equal to the undisturbed output voltage.

Part 3. The results of Part 3 are plotted in Figure 4-8. As was expected, the operating currents were lower due to the mu-metal word lines. The operating range was about the same as on EP_1 and relatively constant for the three sets of word straps.

Of particular significance was the high amplitude of Iw_a. Indications from these tests are that bit densities could be increased significantly without adjacent bit disturb problems by using the mu-metal word straps. A comparison between EP_1 and EP_2 for word line set number 5 is in Table 4-3.

Table 4-3

Plane	Iw_p (ma)	Iw_d (ma)	Iw_a (ma)	Operating Range (%)	E_{out} peak-peak (mv)
EP_1	435	560	428	± 12.5	10.5
EP_2	300	384	845	± 12.5	10.8

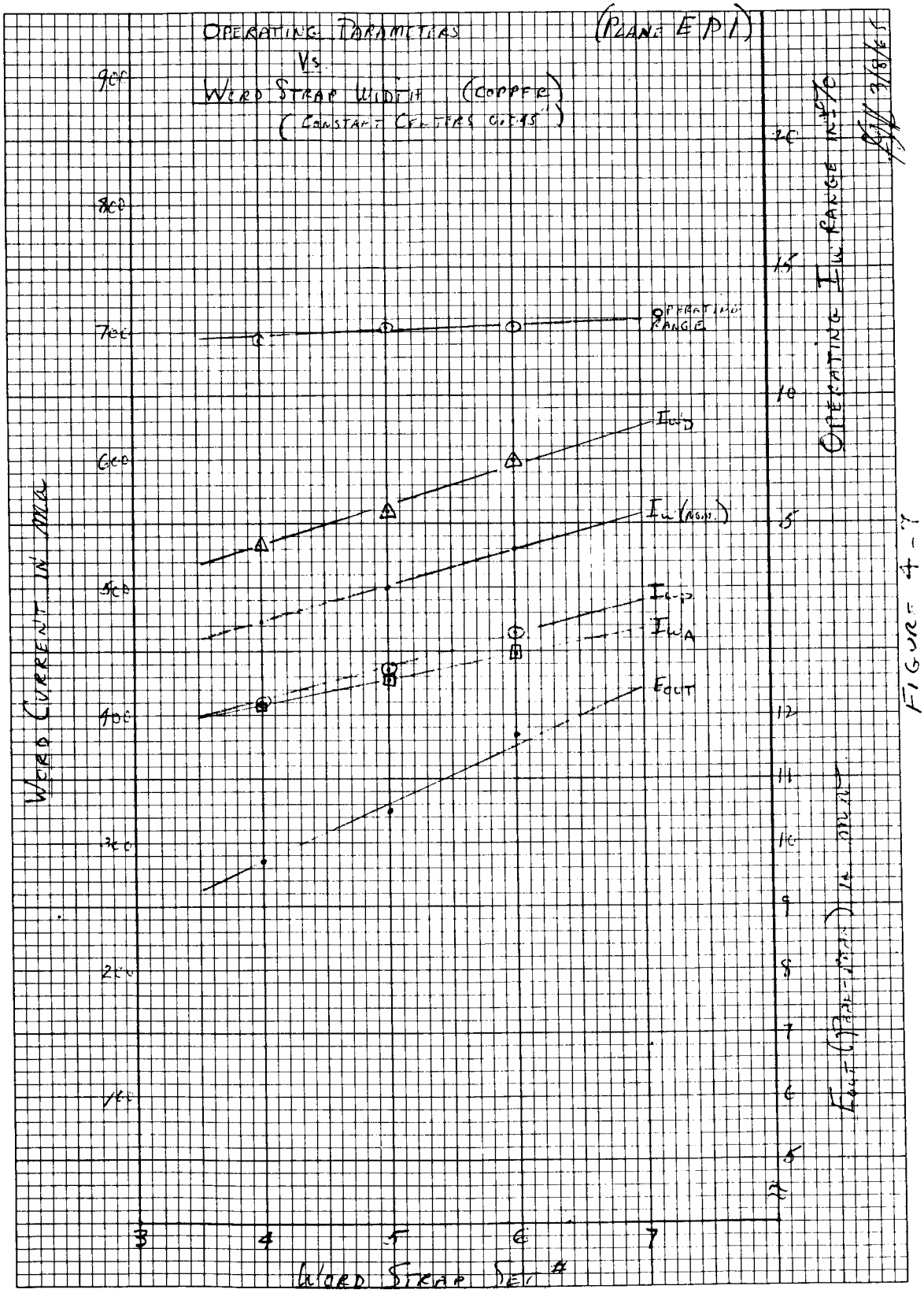

OPERATING PARAMETERS (PLANE EP1)
Vs
WELD STRAP WIDTH (COPPER)
(CONSTANT CENTERS CUTS)
WELD CURRENT IN MA
OPERATING RANGE
$E_{w'D}$
$E_{w(AVG)}$
E_{c-p}
E_{w_A}
E_{OUT}
OPERATING E_w RANGE IN VOLTS
E_{OUT} (PEAK-PEAK) IN VOLTS
WELD STRAP SET #

FIGURE 4-7

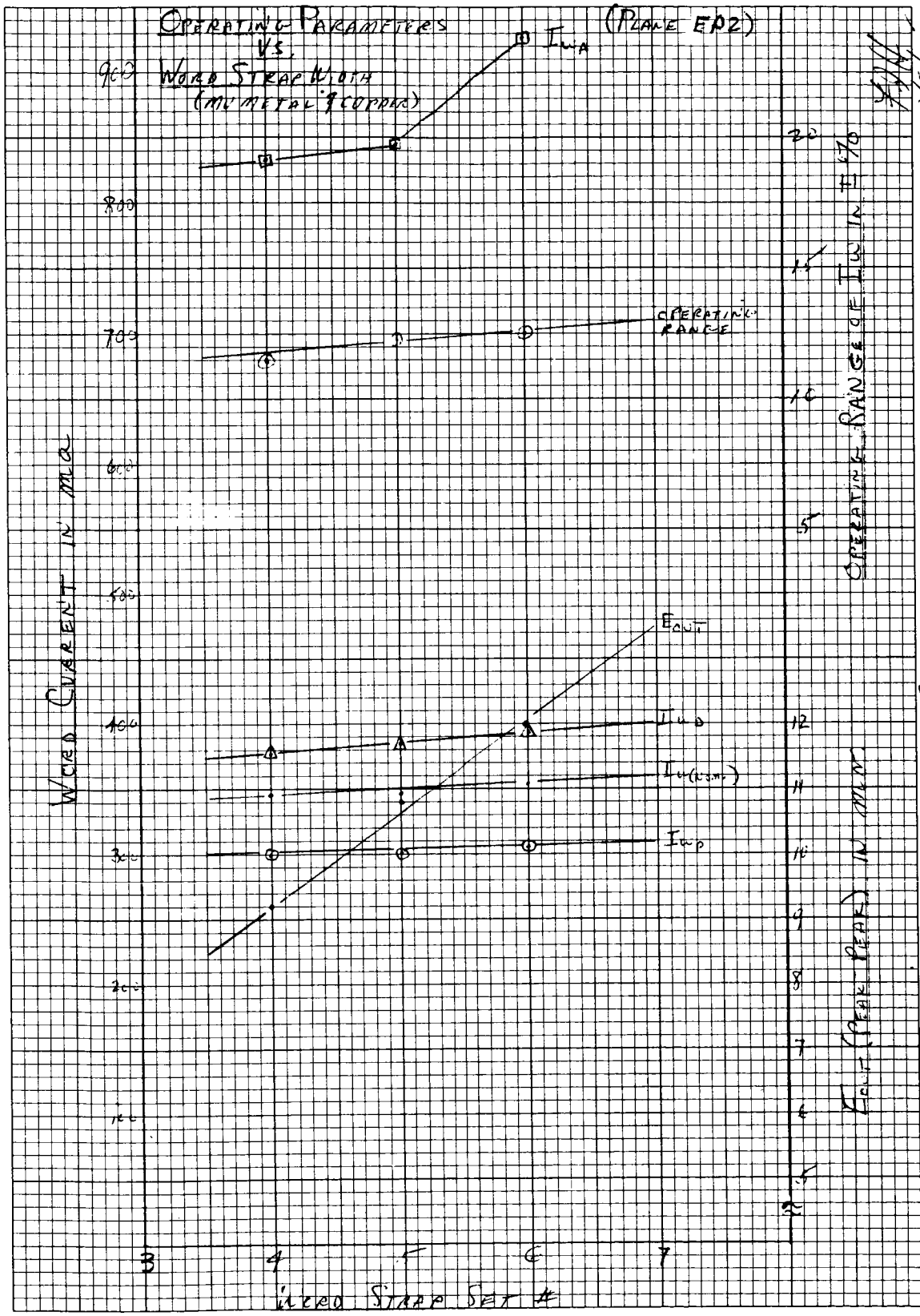

OPERATING PARAMETERS
VS.
WORD STRAP WIDTH
(MV METAL & COPPER)
(PLANE EP2)
I_{w_A}
OPERATING RANGE
E_{cut}
I_{w_D}
$I_{w(bias)}$
I_{w_P}
WORD CURRENT IN MA
WORD STRAP SET #
CUT (PEAK PER) IN MV
OPERATING RANGE OF I_{w_A} IN #'s
3/8/61

FIGURE 4-8

The operating parameters for EP_2 are approximately 30 percent lower than EP_1 while holding the same operating range and output voltages. The nominal operating current of these wires for a single-turn word line is about 720 milliamperes with no adjacent wires and about 930 milliamperes with adjacent grooves filled with wires. Therefore, the nominal operating current was decreased approximately 46 percent with a two-turn copper word line and about 68 percent with a two-turn mu-metal word line.

Part 4. Table 4-4 shows typical results of the test comparing the use of Kovar wire in the adjacent groove to plated wire or an empty groove.

Table 4-4

Contents of Adjacent Groove	Iw_p (ma)		Iw_d (ma)	
	EP_1	EP_2	EP_1	EP_2
Plated Wire	410	281	549	357
Empty	386	271	522	346
Kovar Wire	414	281	555	357

In all cases the effects on Plane EP_1 were greater than EP_2. Also, in Plane EP_2 the parameters Iw_p and Iw_d were always the same with a plated wire as with a Kovar wire. This indicates a strong possibility of eliminating the effect of variation in drive fields due to copper return wires in the memory planes. This could be accomplished by replacing copper with a magnetic wire which would not produce an output signal.

Conclusions of Phase I

The results have indicated that the widest word strap tested is suitable for the Miniature Spaceborne Memory requirement. The signal output voltages can be specified to be a minimum of ±5 millivolts with nominal word currents at about 530 milliamperes. The operating range of a particular set of bits was ±12.5 percent, thereby making a word current tolerance of ±5 percent a realistic figure toward giving reasonable yields of plated wire.

These tests have shown that copper plated mu-metal word lines decrease operating currents, decrease the effect of adjacent bit disturb in random access stores, and increase the uniformity of operating parameters with varying tolerances in the mechanical fabrication of the planes.

The tests with the Kovar wire show that a 5-mil beryllium-copper wire plated with Kovar will provide the desired magnetic characteristics, no output signal and no change in operating currents for adjacent wires. This

provides the exact resistance needed to function as the sense amplifier return wire for transient common mode signal rejection.

The copper plated nickel-iron alloy word lines have been found to be entirely satisfactory. Since this nickel-iron alloy etches faster than the copper, care is required to prevent undercutting. This is done by using a ferric chloride etchant and controlling the etching time.

4.1.2. PHASE II

The investigation of other word line configurations was instigated by a number of factors. A plane using a one-turn word line solenoid is easier to fabricate. Using mu-metal word lines would keep the current requirements in the range of the word-current circuit design. One step further toward easier plane fabrication would be the use of a half-turn word line with a ground plane return. Test results have indicated that adjacent wire noise coupling could also be minimized by using the ground plane return configuration.

Introduction

Four evaluation planes were prepared to perform the tests. The required number of fill wires as found in Phase I, Part 1, were loaded into each plane. EP_1 and EP_2 each contained six sets of single-turn word line solenoids. EP_3 consisted of a 3-ounce copper ground plane with twelve sets of half-turn word lines. Six sets were copper and the other six sets were copper and mu-metal as on EP_2. EP_4 was the same as EP_3 except that the ground plane was made of aluminum 0.005 inch thick. There were three word lines of the same width in each set and all word lines were on a center-to-center spacing of 0.045 inch. The nominal width of each set is listed below. Deviations from the nominal were about ±3 percent.

Set Number	Width (inches)
1	0.013
2	0.017
3	0.021
4	0.025
5	0.030
6	0.035

Procedure

The procedure used in Phase II was the same as for Item 4b of Phase I except for the following variations:

1. In the program for the Iw_a a left adjacent bit history was added. This function was repeated 512 times. The word-current amplitude was the same as Iw_4.

2. In the program for E_{out}, the function A.B.D. was repeated 512 times.

3. Output voltages were recorded with the E_{out} program as listed:

Eo_1 - Read 1

Eo_2 - Read 3

Eo_3 - Read 2 with the A.B.D. function repeated 10^7 times.

4. Data was taken on word strap sets numbers 3 through 6 on EP_3 and EP_4 and on sets numbers 2 through 6 on EP_1 and EP_2.

Results

1. One-turn word line solenoids.

The results of this test are plotted in the Figures 4-9 and 4-10. These curves show that the changes in parameters as a function of word strap width are basically linear. The dip in the output voltage for set number 6, Figure 4-10, might be caused by the narrow guard band between word straps allowing the history pulses to write more flux than the single write function can reverse. A comparison of the shapes of Iw_p and Iw (nominal) shows that between sets number 2 and number 6 there is a change of 22 percent with the copper word lines and 16 percent with the mu-metal word lines.

The slope of Iw_d is greater than the slope of Iw_p in both figures. This might be caused by the uniformity of word field and the method of finding Iw_d.

Table 4-5 shows a comparison of set number 5 for EP_1 and EP_2.

Table 4-5

Plane	Iw_p (ma)	Iw_d (ma)	Iwa (ma)	Operating Range (%)	E_{out} (mv)
EP_1	796	1145	1170	±18	10.5
EP_2	450	620	1900	±16	9.6

Table 4-5 indicates the advantages of using mu-metal word lines. The operating currents are lower, there is no effect from A.B.D., the operating range is about the same and output voltages are equivalent.

A comparison of these results with those using two-turn word lines shows the following:

a. Current amplitudes increased by an expected factor of about 1.6 to 1.8.

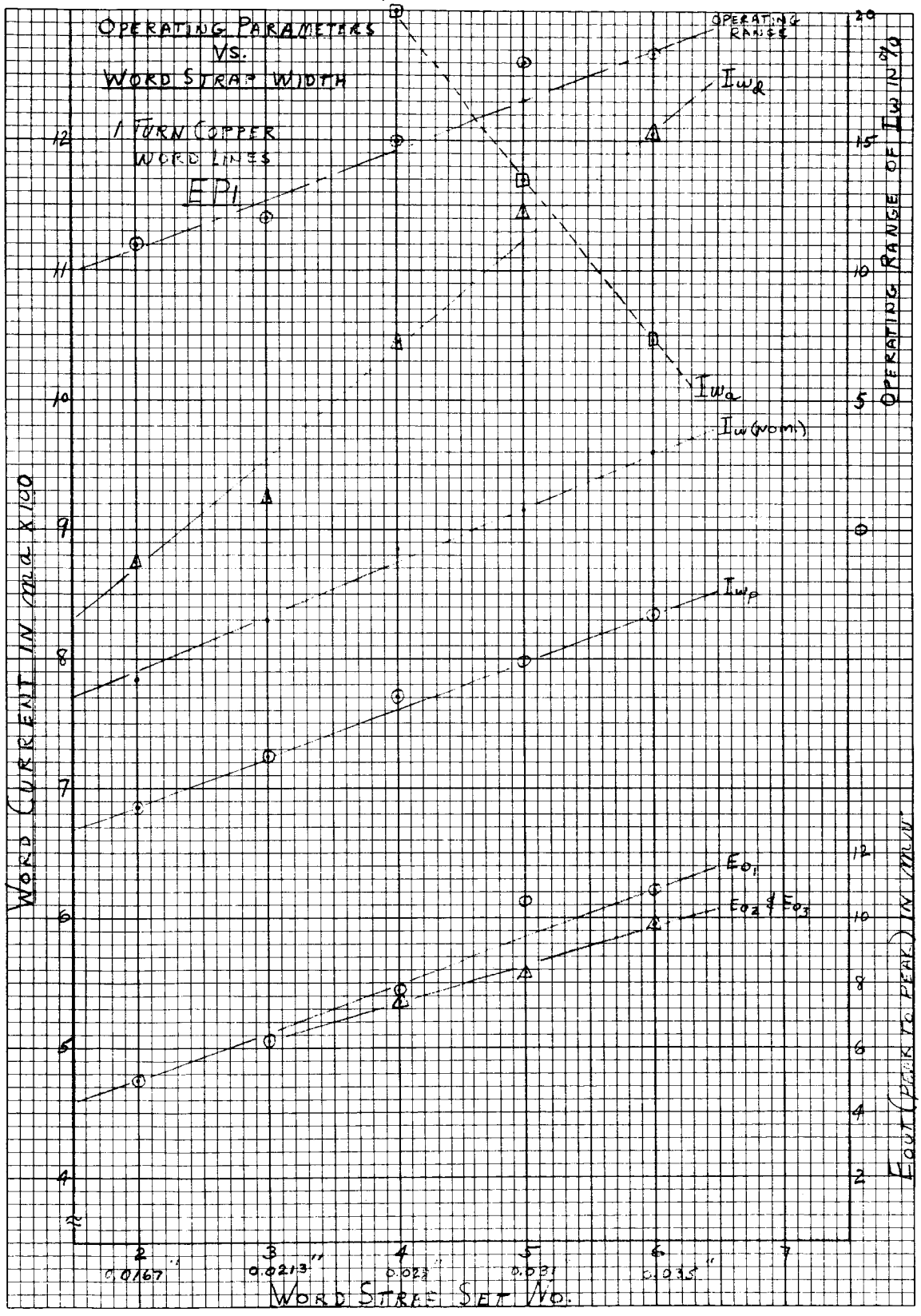

OPERATING PARAMETERS
VS.
WORD STRAP WIDTH
1 TURN COPPER
WORD LINES
EPI
OPERATING RANGES
I_{w_2}
I_{w_1}
$I_{w(nom.)}$
I_{w_3}
E_{o_1}
E_{o_2} & E_{o_3}
WORD CURRENT IN ma X 100
EOUT (PEAK TO PEAK) IN VOLTS
OPERATING RANGE OF I_w IN %
WORD STRAP SET NO.
0.0167"
0.0213"
0.0231"
0.0315"

FIGURE 4-4

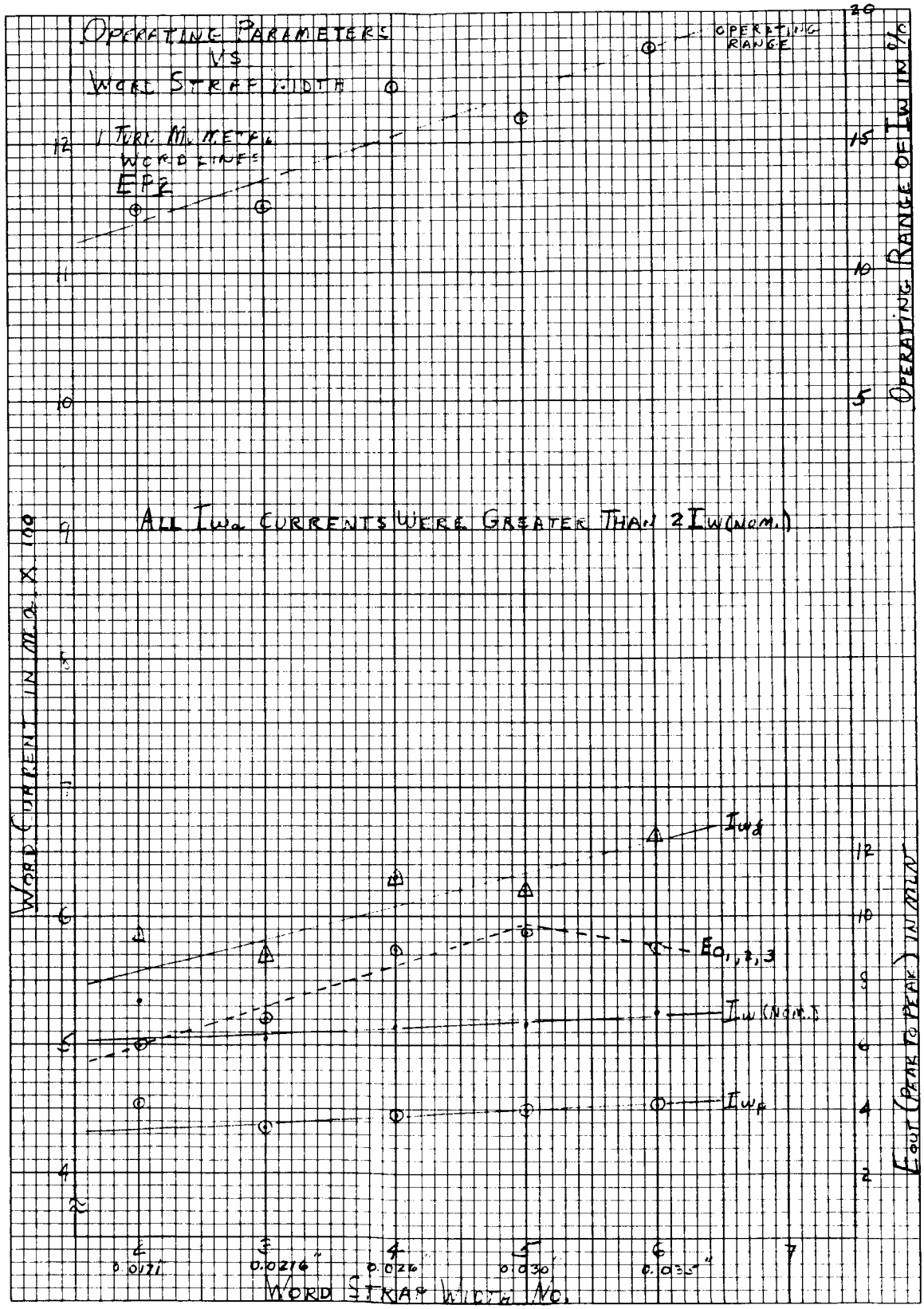

OPERATING PARAMETERS
VS
WORD STRAP WIDTH
OPERATING RANGE
TERMINATED WORD LINES
EPE
ALL Iwa CURRENTS WERE GREATER THAN 2Iw(NOM.)
WORD CURRENT IN mA X 100
OPERATING RANGE OF Iw IN %
Iwd
Eq1,2,3
Iw (NOM.)
Iwp
EOUT (PEAK TO PEAK) IN mV
0.0121"
0.0216"
0.026"
0.030"
0.035"
WORD STRAP WIDTH NO.

FIGURE 4-10

b. The slopes of the curves were greater. Again, this might be caused by the word field differences in uniformity.

c. Output voltages were slightly lower which was probably due to the addition of left A.B.H.

d. Iw_a for the upper lines was much higher which was also due to the addition of left A.B.H. combined with the method of defining Iw_a.

e. The operating range was wider due to the greater slope of Iw_d.

2. Half-turn word lines, copper ground plane (EP_3)

The results of these tests are plotted in Figures 4-11 and 4-12. In general, the performance of the plated wire using EP_3 was not as good as that using EP_1 or EP_2. Variations of the parameters with word strap width were not as smooth. As before, the mu-metal word lines showed operating advantages over the copper word lines. A comparison is shown in Table 4-6 for set number 5.

Table 4-6

Word Lines	Iw_p (ma)	Iw_d (ma)	Iw_a (ma)	Operating Range (%)	E_{out_1} (mv)
Copper	1320	>1800	1120	±17.5	20
Mu-metal	705	1030	715	±18.8	12

The high outputs (Eo_1) with copper word lines is an indication of the word field spreading which occurs when using the copper ground plane return. This is further exhibited by the effect on Eo_2 and the complete reversal of Eo_3. The mu-metal word lines tend to confine the field and the effect on Eo_2 and Eo_3 is less severe.

On both figures Iw_a is nearly equal to or is less than Iw_p. Because of this, the A.B.D. was able to decrease or reverse the flux written in the B.U.T. However, indications are that this was the result of field spreading and not involved with the creep phenomenon.

3. Half-turn word lines, aluminum ground plane (EP_4)

The results of this test are plotted in Figures 4-13 and 4-14. Iw_a and Eo_3 measurements were omitted from these tests.because they are not applicable to this sequential buffer memory.

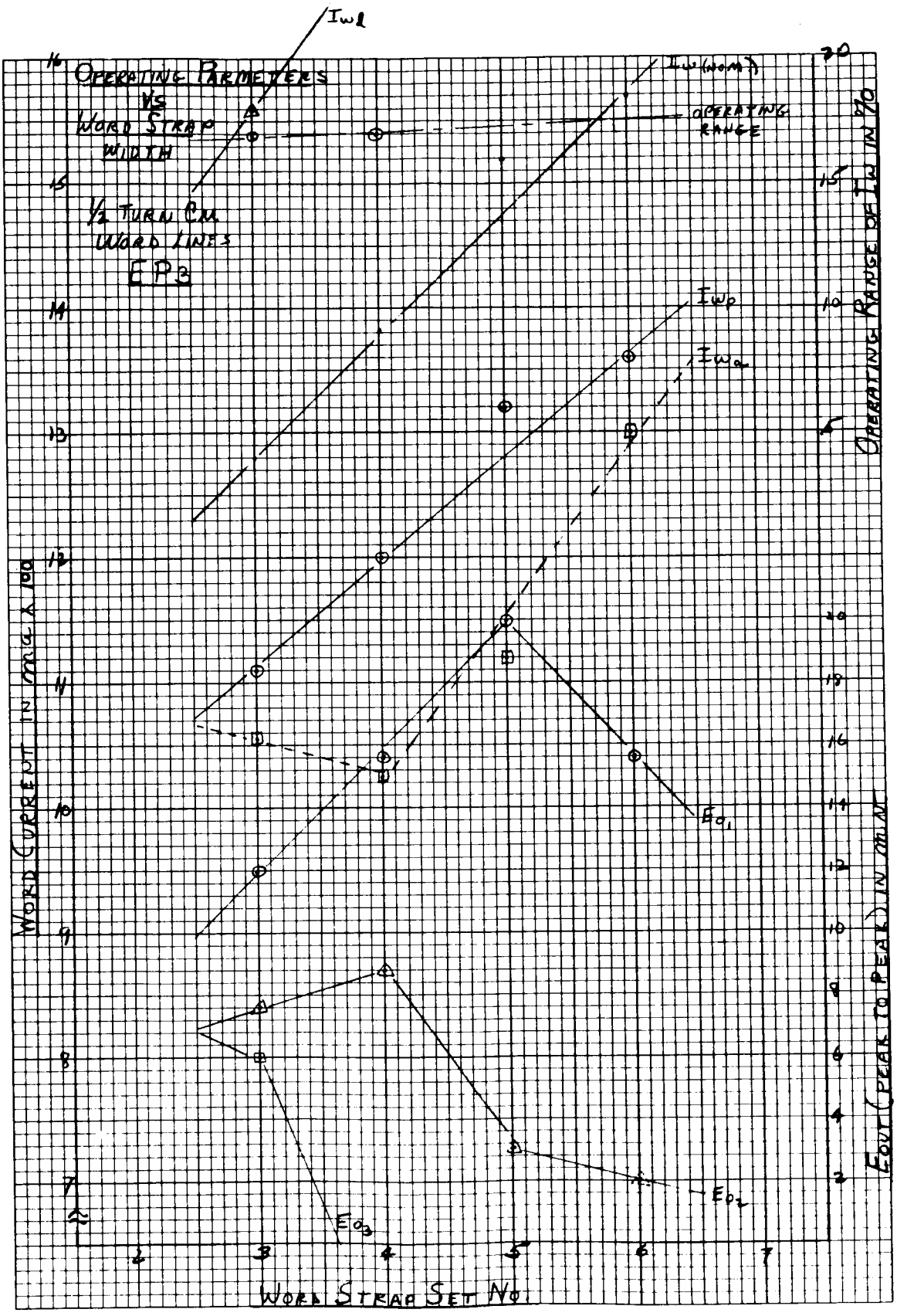

OPERATING PARMETERS
VS
WORD STRAP
WIDTH
½ TURN CU
WORD LINES
EP3
I_{w1}
$I_{w(nom)}$
OPERATING RANGE
I_{wp}
I_{w2}
E_{o1}
E_{o2}
E_{o3}
WORD CURRENT IN mA x 10
EOUT (PEAK TO PEAK) IN mV x 10
WORD STRAP SET NO.

FIGURE 4-11

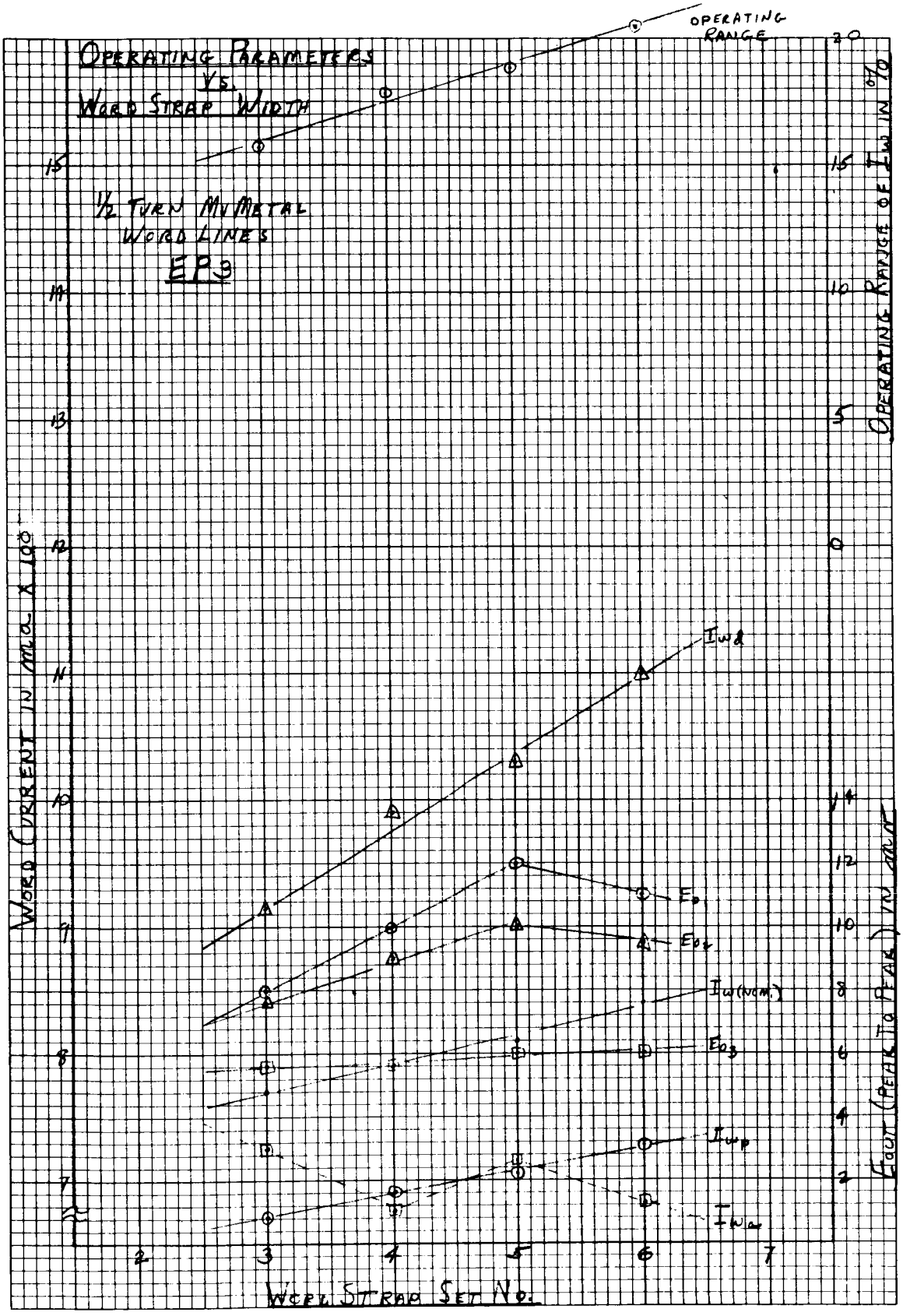

OPERATING PARAMETERS
VS.
WORD STRAP WIDTH
½ TURN MuMETAL
WORD LINES
EP3
OPERATING RANGE
WORD CURRENT IN mA x 10
OPERATING RANGE OF Iw IN %
EQUIV (PEAK TO PEAK) VOLTAGE
Iw8
Eo1
Eo2
Iw(NOM.)
Eo3
Iwo
Iw0
WORD STRAP SET NO.

FIGURE 4-12

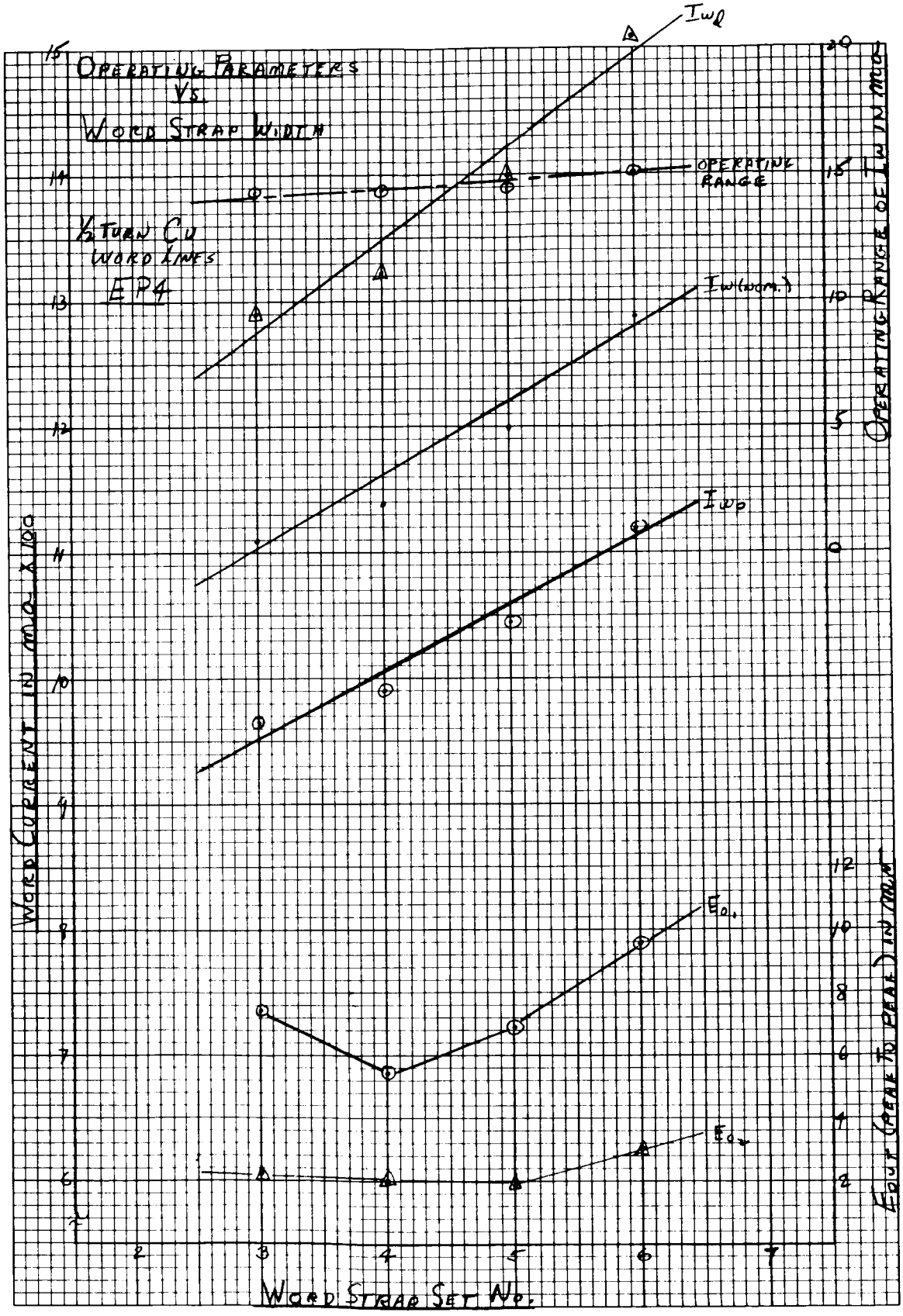

OPERATING PARAMETERS
VS.
WORD STRAP WIDTH
½ TURN Cu
WORD LINES
EP4
I_{WL}
$I_{W(nom.)}$
I_{WP}
E_{O_1}
E_{O_2}
OPERATING RANGE
WORD CURRENT IN mA x 100
EOUT (PEAK TO PEAK) IN mV
OPERATING RANGE OF IW IN mA
WORD STRAP SET WP.

FIGURE 4-13

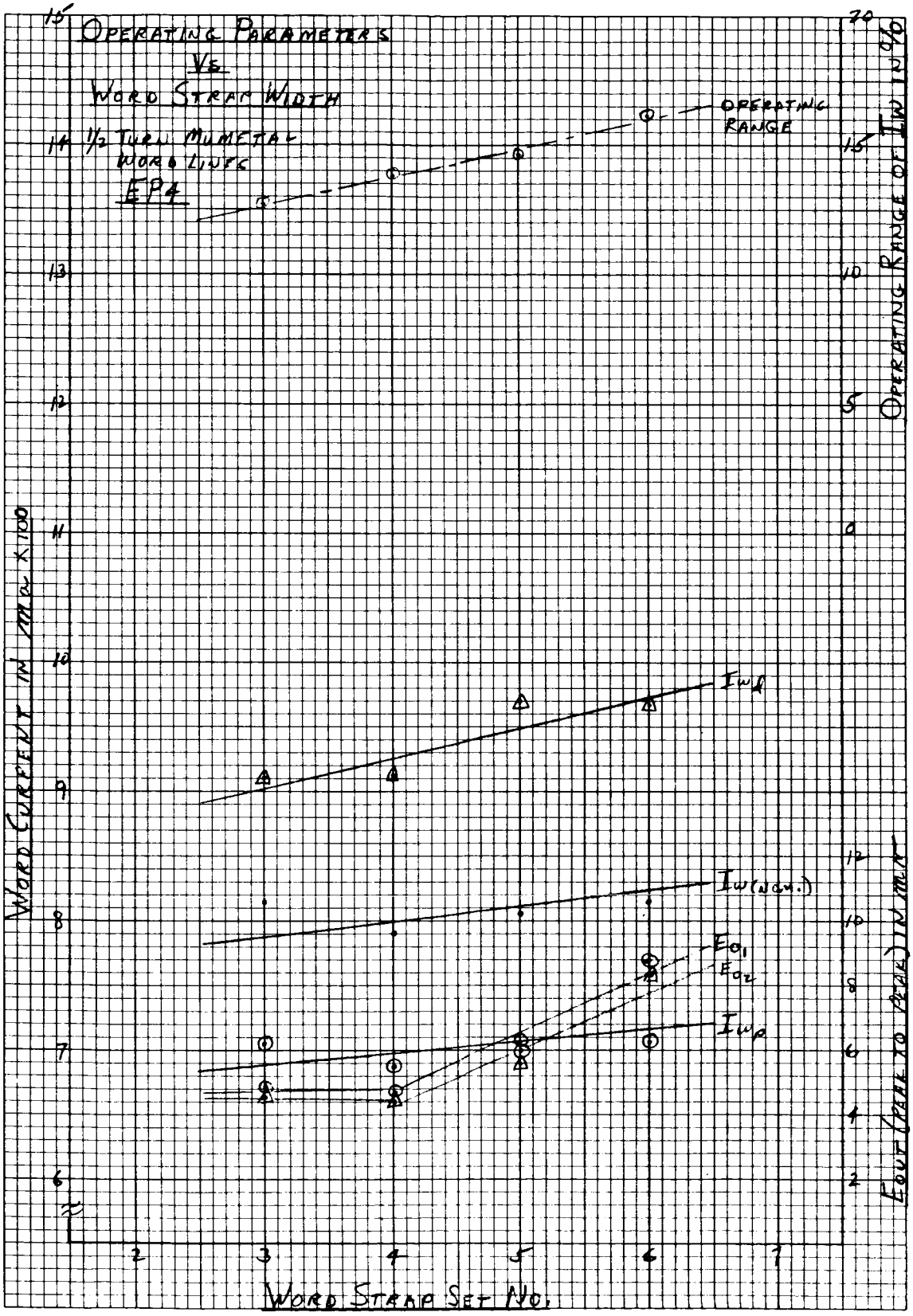

OPERATING PARAMETERS
VS.
WORD STRAP WIDTH
1½ TURN MUMETAL
WOUND LINKS
EP4
OPERATING RANGE
WORD CURRENT IN mA x 100
OPERATING RANGE OF Iw IN %
Iw1
Iw(wdw.)
Eo1
Eo2
Iwp
WORD STRAP SET NO.

FIGURE 4-14

The results of the tests on EP_4 were expected to be similar to those on EP_3. However, both the current amplitudes and output voltages were lower, but the difference between Eo_1 and Eo_2 was much less. Also, the overall performance of EP_4 looked better. A comparison between copper and mu-metal word lines (EP_4) set number 5 is in Table 4-7.

Table 4-7

Word Lines	I_{wp} (ma)	I_{wd} (ma)	Operating Range (%)	E_{out_1} (mv)
Copper	1045	1400	±14.5	6.9
Mu-metal	705	970	±14.6	6.0

Conclusion

The table of operating parameters is reproduced below for reasons of an overall comparison.

Table 4-8

Plane	Word Line*	I_{wp} (ma)	I_{wd} (ma)	I_{wa} (ma)	Operating Range (%)	E_{out_1} (mv)
EP_1	2 TC	435	560	428	±12.5	10.5
EP_2	2 T MM	300	384	845	±12.5	10.8
EP_1	1 TC	796	1145	1170	±18.0	10.5
EP_2	1 TMM	450	620	>900	±16.0	9.6
EP_3	½ TC	1320	>1800	1120	±17.5	20.0
	½ T MM	705	1030	715	±18.8	12.0
EP_4	½ TC	1045	1400	—	±14.5	6.9
	½ T MM	705	970	—	±14.6	6.0

*T = Turns, C = Copper, MM = Mu-metal

The curves plotted in Figures 4-7 through 4-14 and the results listed in Table 4-8 show that the best overall performance of the plated wire is attained using the two-turn mu-metal solenoid word lines. However, because of memory considerations, the ground plane configuration is more desirable. On either EP_3 or EP_4, the mu-metal word lines required current amplitudes in a reasonable range and allowed operation with wider word straps than the copper word lines. EP_3 had wider operating ranges and higher output voltages, but appeared more susceptible to word field spreading than EP_4.

The memory planes will be made of 5-mil thick aluminum sheets bonded to an aluminum honeycomb core. This frame serves as the structural support and the electrical ground for the memory.

4.2. CORROSION PROTECTION OF PLATED WIRES

Protective overplating, using tin, gold and rhodium, was tried to protect the magnetic film from corrosion. It was found that the protective coating tends to be damaged by contact with the mercury cups used to make electrical contact with the wires during manufacture. It was also found that a pinhole-free coating was imperative, and that coating sufficiently thick to be free of pinholes reduced the magnetic output of the wires. Damaged or pin-holed coating proved to produce more corrosion in wires than was seen in uncoated wires.

A study of various methods of cleaning showed that if the wires are wiped with alcohol-soaked tissues, the Nickel-Iron magnetic film possesses, by itself, sufficient corrosion resistance when used inside the H-film-teflon-tunnel structure. Wires cleaned in this manner resisted corrosion successfully after an exposure of 1417 hours to a 95°C and 85 percent relative humidity atmosphere. The conclusion is that there should be no corrosion problems provided the wires are properly cleaned.

Refer to Appendix IV for a detailed discussion of methods which were tried to provide corrosion protection of plated-wire memory elements.

4.3. LIFE TESTS

Life tests have been conducted on the UNIVAC plated-wire memory element at elevated temperatures and under simulated and actual operating conditions. These tests indicate that the magnetic characteristics of the plated wire are stable as manufactured. Under certain conditions, never experienced in a memory, the values of H_k (the anisotropy field) and H_c (the wall motion coercive force) will drop.

Two memory planes, containing 768 bits each, were installed in a small buffer memory system. The planes were operated continuously for more than a thousand hours each at a temperature of 75°C to 80°C. The allowable variations of the operating currents for error-free operation were essentially unchanged. The duty factor of the word drive current (which generates the transverse drive field) was 2.6×10^{-5}. This is ten times larger than the maximum continuous duty factor in the 1.4×10^6 bit memory, 2.7×10^{-6}. The 1000-hour tests were therefore roughly equivalent to 10,000 hours of actual operation because of this duty factor.

Life tests conducted under simulated operating conditions have shown the following:

1. Changes in magnetic properties occur only when dc transverse drive fields are applied in conjunction with high temperatures.

2. DC transverse drive fields or high temperatures applied separately do not cause changes.

3. The temperature needs to be +55°C to +60°C or higher to observe these changes.

4. Pulsed transverse drive fields of 10 percent duty-factor and +80°C temperatures have not caused changes after 350 hours whereas different sections of these same wires subjected to dc fields have had measurable changes in 16 hours.

5. Magnetic annealing of the plated wires prevent changes in magnetic properties even with dc fields and high temperature applied.

Conclusions

A. A change in transverse-field duty factor from 100 percent to 10 percent extends the life more than 20:1.

B. The operating life tests and conclusion A indicate that magnetic annealing is not needed for any memory with duty factor less than 10 percent and continuous temperature of +80°C and less.

Actions being taken

Additional life tests will be made under operating conditions with duty factors at least ten times larger than those actually encountered. It is planned to accumulate 40 x 10^6 memory element-hours of life test over a 14-week period. This life test will be performed using a memory plane built like the final design and containing approximately 10,000 memory elements that have not been magnetically annealed and another 10,000 memory elements that have been magnetically annealed. The elapsed time of 2000 hours that is planned should be roughly equivalent to 20,000 hours of actual life because the duty factor of the word drive field will be ten times greater than the operating condition. This then approximates 2.3 years. It is planned to magnetically anneal all wires in the engineering model memory until more data becomes available to review the decision.

SECTION 5

MEMORY PACKAGING AND INTERCONNECTIONS

The contract requires that it be conclusively shown that the 2.8 x 10^{-6}-bit memory could be packaged into a Nimbus box 6 inches by 8 inches by 13 inches. The engineering model to be built during phase II will be a 1.4 x 10^{6}-bit half-memory. The two halves making up the full memory are electrically and physically independent. Therefore the goal is to show that the half-memory will fit into a box 6 inches by 4 inches by 13 inches.

The proposed circuit packaging for a maximum density is relatively well known, and designs and calculations only will be used to show the volume required. The memory stack design is, relatively speaking, much newer, and it was decided to make the stack design in final size. Therefore all the packaging design work in phase I was concerned with the selection of materials and fabrication techniques for the memory stack.

5.1. PACKAGING SUMMARY

Phase I of the contract was completed as scheduled; the following milestones were satisfactorily completed:

1. Materials were evaluated and selected for utilization in the program.

2. The memory planes and stack were designed and developed with respect to the environmental requirements presented in the statement of work.

3. Applicable drawings were prepared to reflect the final design.

4. One operating memory frame was fabricated to reflect the tentative design for the entire package.

5. A mock-up of one-third of the 1.4-million-bit memory stack was fabricated; this mock-up reflects the entire stack configuration.

6. A materials report was published describing the results obtained from tests performed on materials to be utilized in the end product.

5.2. HYBRID CIRCUITS

Five circuits that are used in reasonable quantity (85 percent of total circuits) were designed and are being built in hybrid form. The low-level switch matrix P-HC-03 uses chip semiconductors and thin-film (tantalum or nichrome) resistors. Six switches are mounted in one 0.25-inch-by-0.25-inch flat pack.

The other circuits use discrete cased semiconductors and screened ceramic resistors. To minimize cost, these circuits were not made in their smallest size and use discrete cased semiconductors in place of chips.

The objective of this approach is to show that all circuits will work satisfactorily in this construction. A future change for packaging a prototype in minimum volume would use chip semiconductors in place of the discrete cased units. No electrical redesign would be needed since no changes would have been made affecting the performance. Specifications for these circuits are given in appendix III.

5.3. GLOSSARY

Word Drive Line: A strip of printed wiring bonded to a sheet of Kapton* film. The word line material is copper-plated shield Mu.

Word Line Overlay: The group of parallel word lines attached to the base material (Kapton).

Plated Wire Carrier: A composite film containing tunnels for housing plated wires. The carrier is composed of Kapton/Type H F film.

Word Line Solenoid: The assembly of the word line overlay bonded to the plated-wire carrier. These units are bonded in such a way as to enable the parallel word lines to cross the parallel tunnels in the plated-wire carrier at right angles. The two units are bonded together with a film adhesive in a thermal press and thus produce the required solenoid.

Plated Wire: A beryllium copper wire with a magnetic plating.

Memory Plane: A laminated structure composed of a word line solenoid bonded to a copper or aluminum alloy ground plane. Plated wires are contained in the plated-wire carrier to complete the assembly.

One bit of information can be stored at each intersection of a word line and a plated wire. This means that the bit capability of any plane is simply the number of word lines times the number of plated wires (assuming every word line crosses every plated wire).

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*Kapton-DuPont Registered Trademark

Memory Stack: A group of interconnected memory frames. Plated wires which are parallel to and adjacent to each other in adjacent frames are connected electrically. This provides for a series of parallel wires passing through each frame of the entire stack.

Memory Frame: A combination of two memory planes, one mounted on each side of a ground plane. The plated wire side of the memory plane is bonded to the surface of the ground plane. The metal plane described under heading 5.8 is the structural support of the memory frame. The ground plane is a laminated honeycomb structure. The structure provides a stiff support for the memory and is light weight, thus compatible with spacecraft design.

Basic Testable Element: An element which combines a memory frame with a structural spacer. The spacer also serves to support the transition strip utilized for outer-frame plated wire connections. This assembly is the one which will be subjected to the life-test environment and which will provide the necessary life-test data needed to satisfy the contract.

5.4. MECHANICAL DESIGN

5.4.1. THE DESIGN CRITERIA APPLICABLE TO A MEMORY PLANE

The following is a list of design criteria applicable to various components and materials:

1.	Bit capacity:	69,120
2.	Word drive lines:	98 (including 2 spares)
3.	Plated wires:	730 (including 10 dummies and 80 return wires)
4.	Word drive line construction	
	Material:	Copper-plated shield Mu 30
	Nominal Dimensions:	$.034\ ^{+000}_{-003}$ on 0.44 centers
	Configuration:	Half-turn word line
5.	Switches on plane:	4 (each consists of transistor and resistor)
6.	Diodes:	120 (supplied 5 in a molded module [24 required]).

It should be noted that the basic testable element in the memory is the memory frame. To form a testable element, the plated wire is preformed into a hairpin configuration and fed into both memory planes simultaneously.

5.4.2. ENVIRONMENTAL DESIGN CRITERIA

The following is a list of the applicable operating environments which the memory design reflects, to satisfy the contract requirements:

1. Temperature. The memory shall be capable of nondegraded performance over the temperature range of minus (-) 20°C to plus (+) 80°C. It shall survive storage temperature of plus (+) 150°C for 48 hours.

2. Vacuum. The memory shall be designed to operate unsealed under conditions of near Earth or interplanetary-space environment at pressures of 10^{-11} mm of H_g or less.

3. Humidity. The memory shall be designed to operate under conditions of relative humidity up to 100 percent with the resulting condensation of water or frost.

4. Vibration. The design of the memory shall be such that a packaged prototype will operate through the launch environment. The required vibration is specified in the enclosed environmental specification.

5. Test Environment. Since a prototype of this memory will be used in the laboratory and tested there and in a spacecraft by many different types of personnel, it is important that protection be provided in case of accidental shorting of exposed connections. This feature shall be demonstrated in the 1.4×10^{-6}-bit model.

5.4.3. MECHANICAL CONFIGURATION OF ENTIRE MEMORY PACKAGE

Appendix V, "Materials Report Number 1", contains a drawing, "Memory Stack, SK 1006" which describes the external configuration and also the areas allotted for the various subassemblies within the package.

A tentative selection of all materials to be utilized on this program has been accomplished. These materials have been selected because of their capability to meet the mechanical and electrical requirements of this package. A complete report with respect to the materials selected is contained in Appendix V, designated "Materials Report Number 1". The estimated weight of a prototype memory system of 2.8×10^6 bits is 35 to 37 pounds.

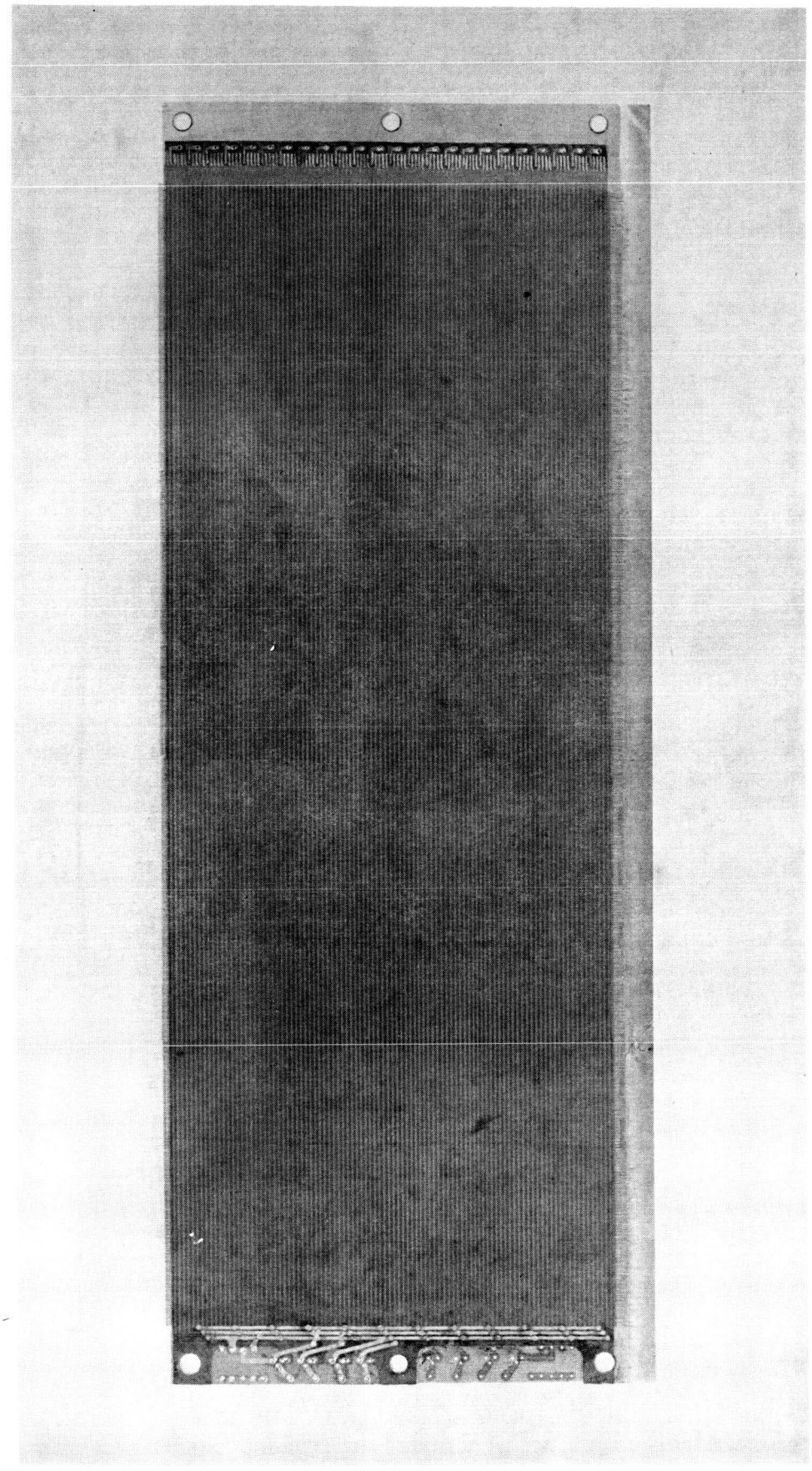


Figure 5-1. Miniature Spaceborne Memory Frame Side 1

5.5. MEMORY FRAME DETAIL

Figure 5-1 reflects the overall configuration of the memory frame. The assembled unit consists basically of a ground plane with memory solenoids bonded to each side.

The ground plane is a laminated structure consisting of copper surfaces, aluminum alloy frame and aluminum alloy honeycomb bonded together with a glass cloth reinforced film adhesive. The ground is bonded at 350°F, 200 psi, for a duration of 1 hour. This results in a light-weight, rigid, flat-surfaced support for the word line solenoids.

The word line solenoids (2 required) are prefabricated and bonded to the ground plane with a film adhesive. Subsequent assembly consists of placing the U shaped plated wires into the appropriate tunnels in the plated wire carrier. The U portion of the plated wire is supported and protected by a molded comb which is bonded along the side of the frame. The A and B switch electronic parts are then assembled and soldered in place. Referring to Figure 5-2, the B switches, consisting of a transistor and resistor for each switch, are evident on the top frame of the stack. At the opposite end of the word drive lines, one diode network can be seen assembled and soldered to the appropriate word lines.

5.6. MEMORY STACK

Figure 5-2 depicts one-third of the total 1.4-million-bit memory stack. This figure was taken of a conceptual model closely approximating the final configuration. It can be seen that the individual memory frames are sandwiched together and interconnections between the frames accomplished while sandwiched.

Figure 5-3a shows the end of the stack where the A-switch inputs pass through the diode packages. The figure demonstrates the sandwiched construction and shows the approximate location of the diode packages. Figure 5-3b is a view of the B-switch end of the word drive lines. The eight switches per frame are evident in the figure and the packaging density at this location can be seen to be very high due to the allowable external dimension of the package.

Figure 5-4a shows the edges of the frames with a section of combs in place. These combs protect and support the U-shaped plated wire. Figure 5-4b demonstrates the connection technique utilized to provide a continuous plated wire from frame to frame. The adjacent (frame to frame) plated wires are soldered to formed transition strips bonded to the stack spacers (located between memory frames). The transition strip contains flexible printed wires located on center lines spaced at 0.015-inch intervals along the edge of the planes. The plated wires are therefore soldered to these pads to complete the assembly.

Figure 5-5 is an assembly drawing (SKAP1087) of the Plane Assembly. This drawing provides further details of the memory frame assembly.

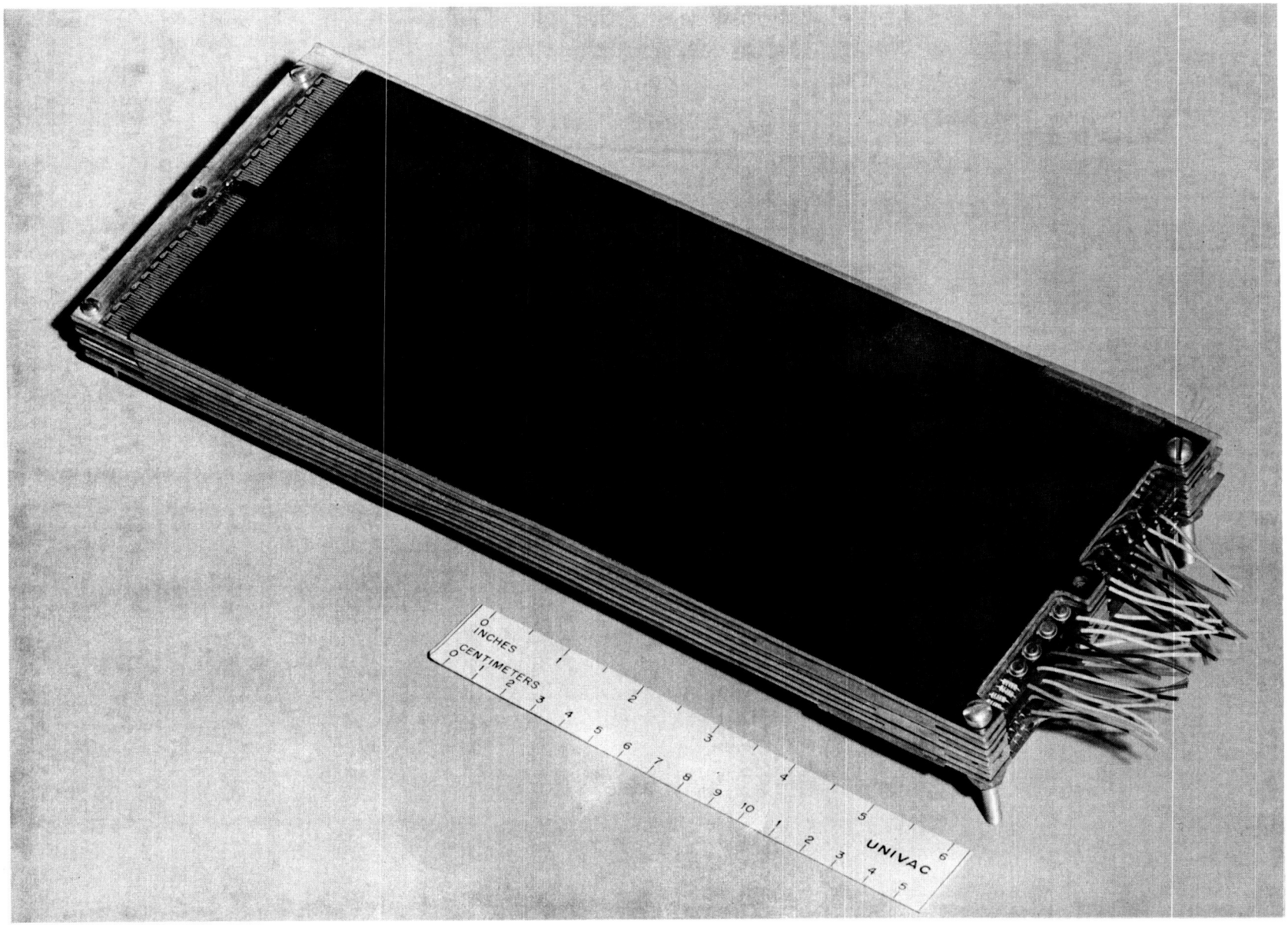


Figure 5-2. Miniature Spaceborne Memory Stack

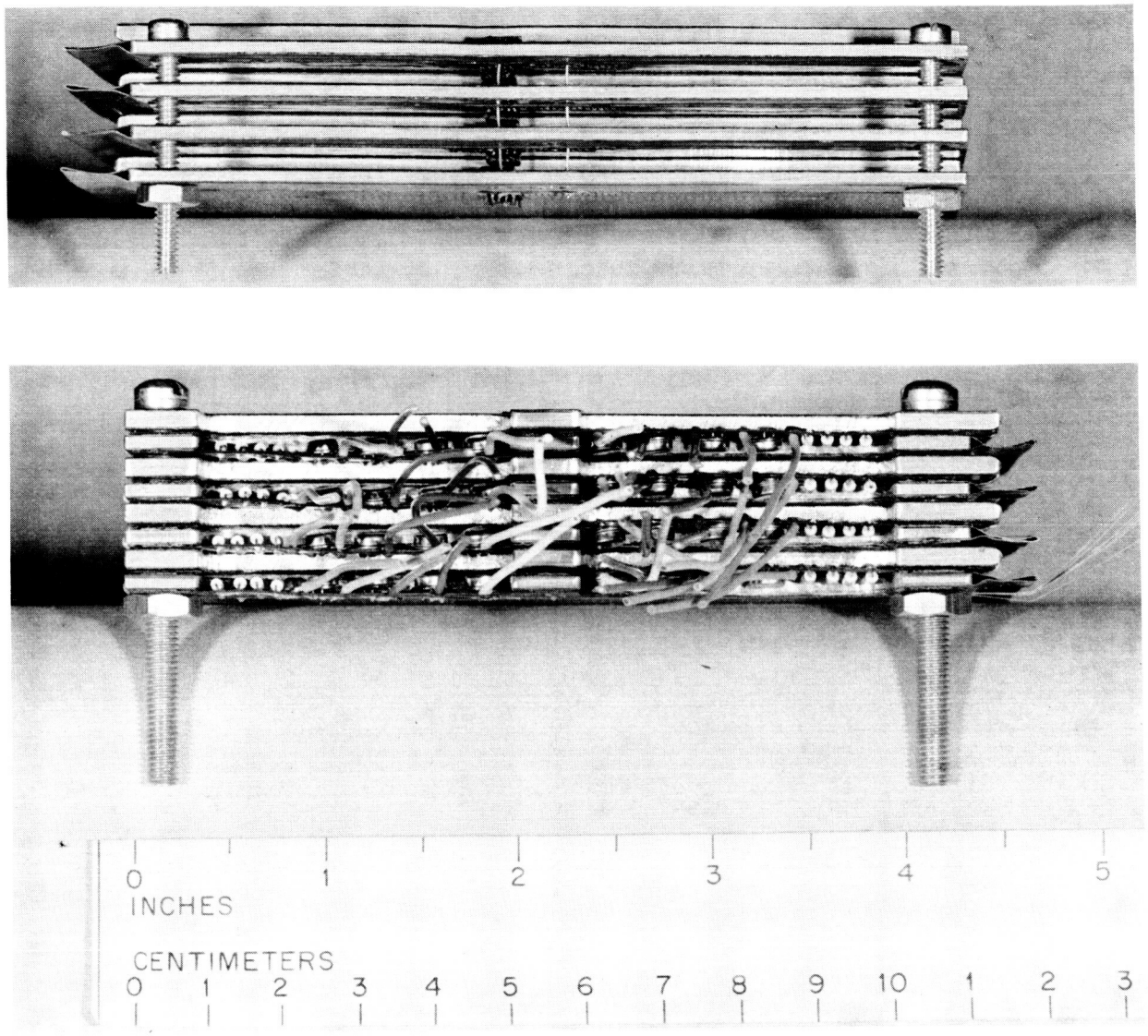


Figure 5-3. Miniature Spaceborne Memory Stack (end views)

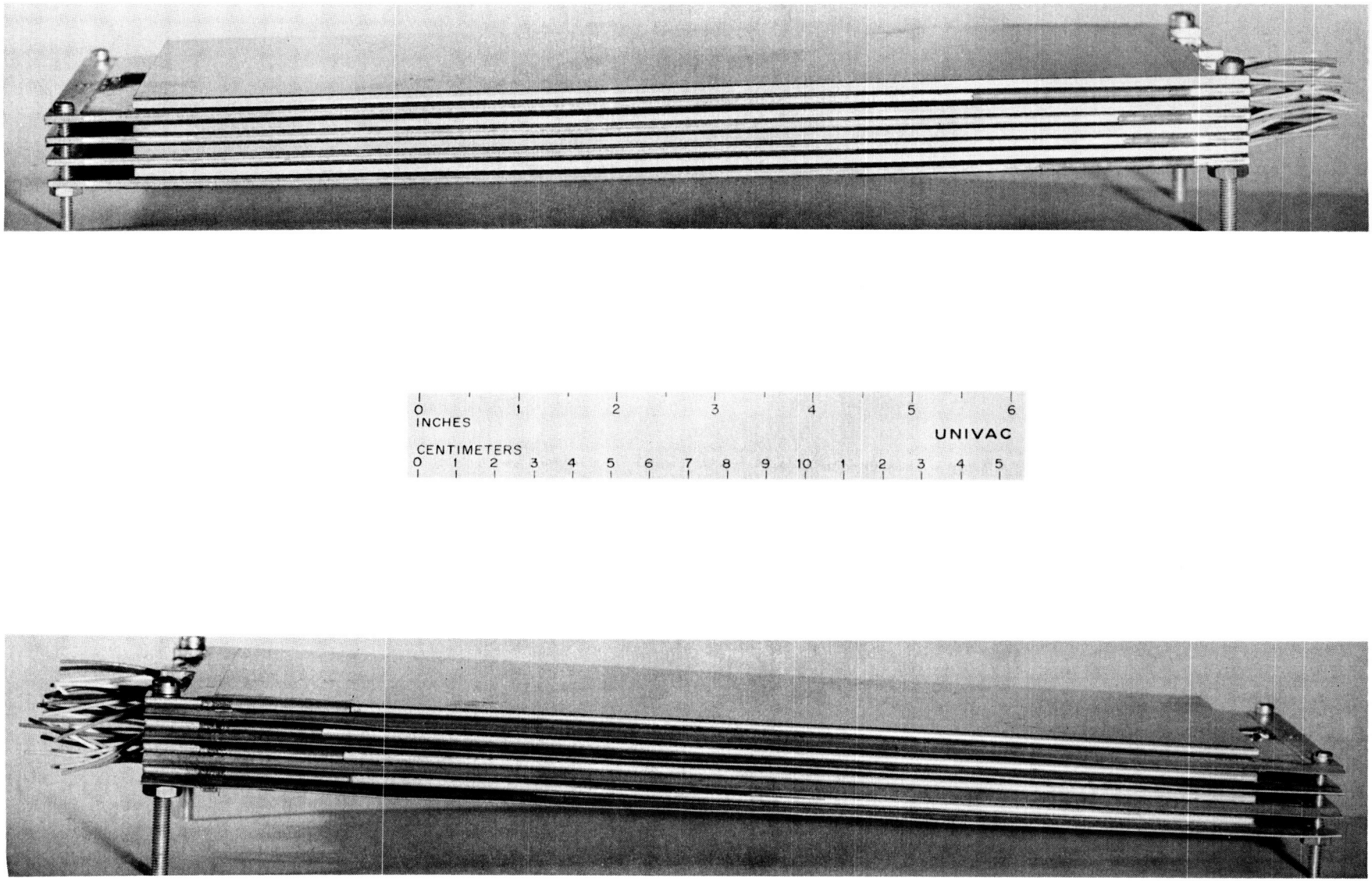
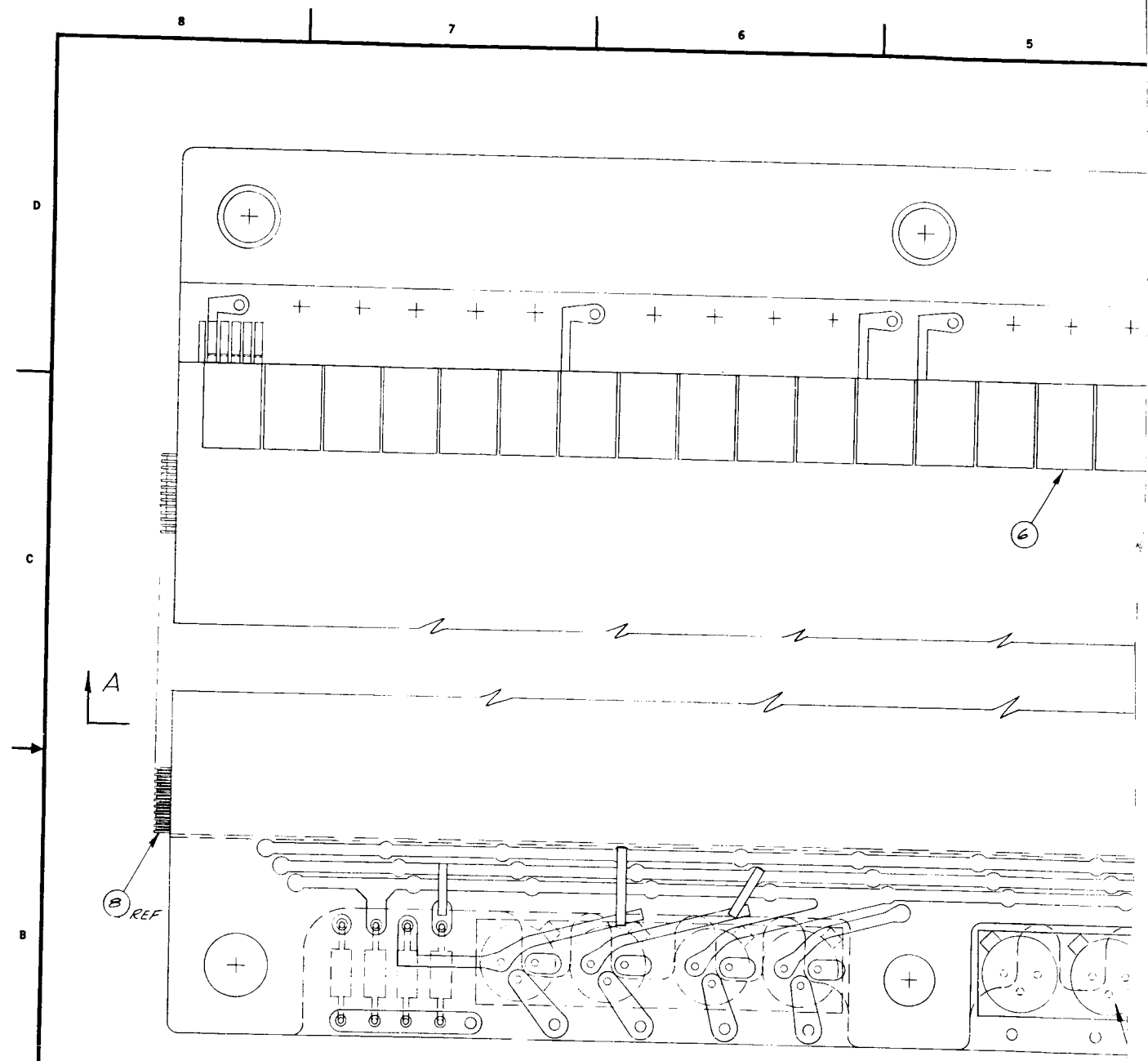


Figure 5-4. Miniature Spaceborne Memory Stack (edge views)



SPACER ASSY NOT SHOWN
FOR CLARITY

2

REVISIONS						
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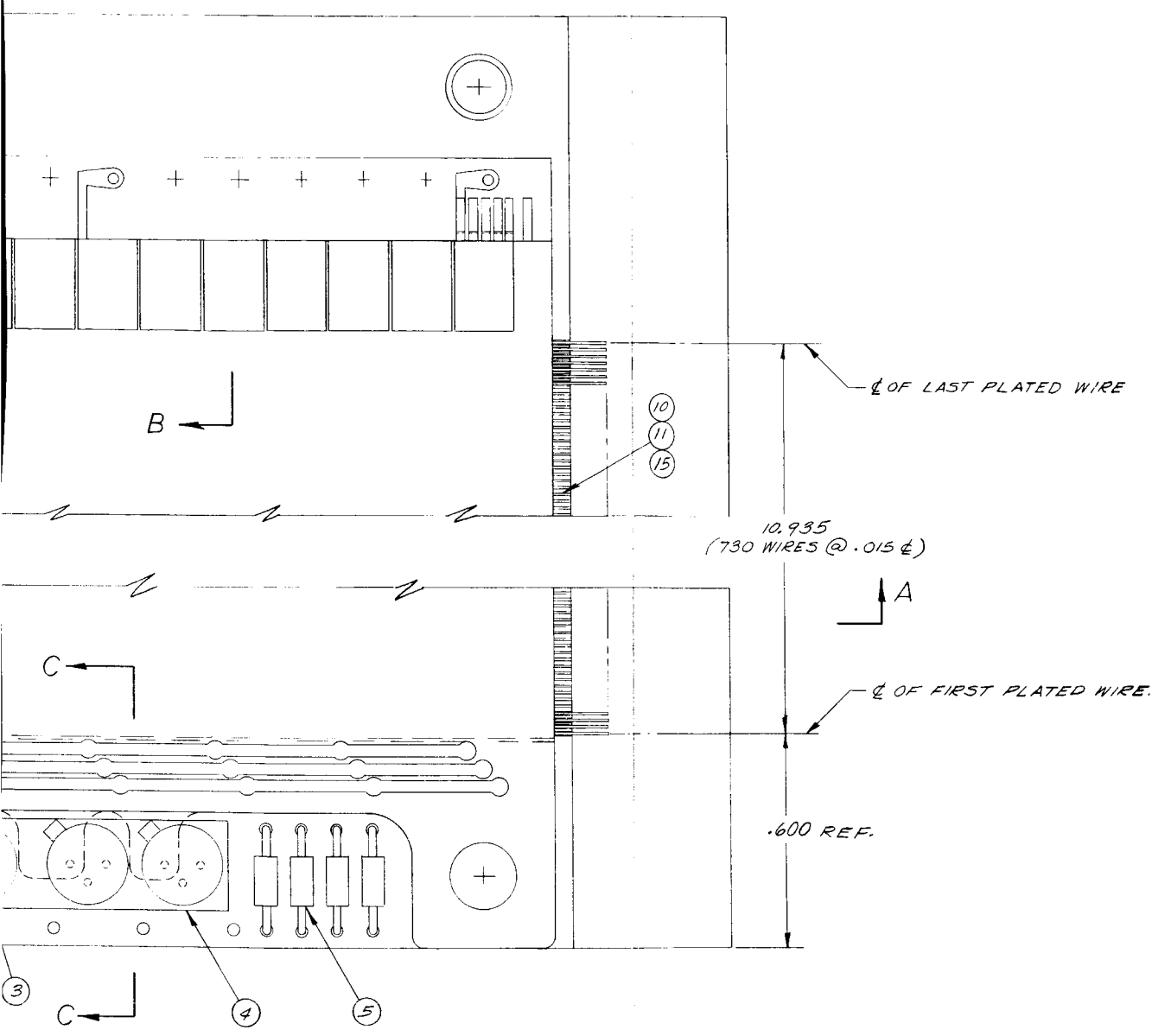

QTY REQD	FIND	REF DES	CODE IDENT	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIAL

PART NO.
IDENT. NO.

NEXT ASSY | EQUIPMENT
APPLICATION
COMMODITY CODE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES. TOLERANCE ON
2 PLACE DECIMALS ± | 3 PLACE DECIMALS ± | ANGLES ±
HOLE DIAMETER TOLERANCE
0 THRU .250 +.003 −.002 | .251 THRU .500 +.005 −.003 | .501 & LARGER +.010 −.005
THREADS: EXT CL 2A, INT CL 2B
MATERIAL
FINISH

		DATE
LAYOUT	G. KAMINSKY	7.1.65
DRAFTSMAN	G. Kaminsky	7.1.65
CHECKER		
ENGINEER	R. HOFFMAN	
APPROVAL		

CLASS

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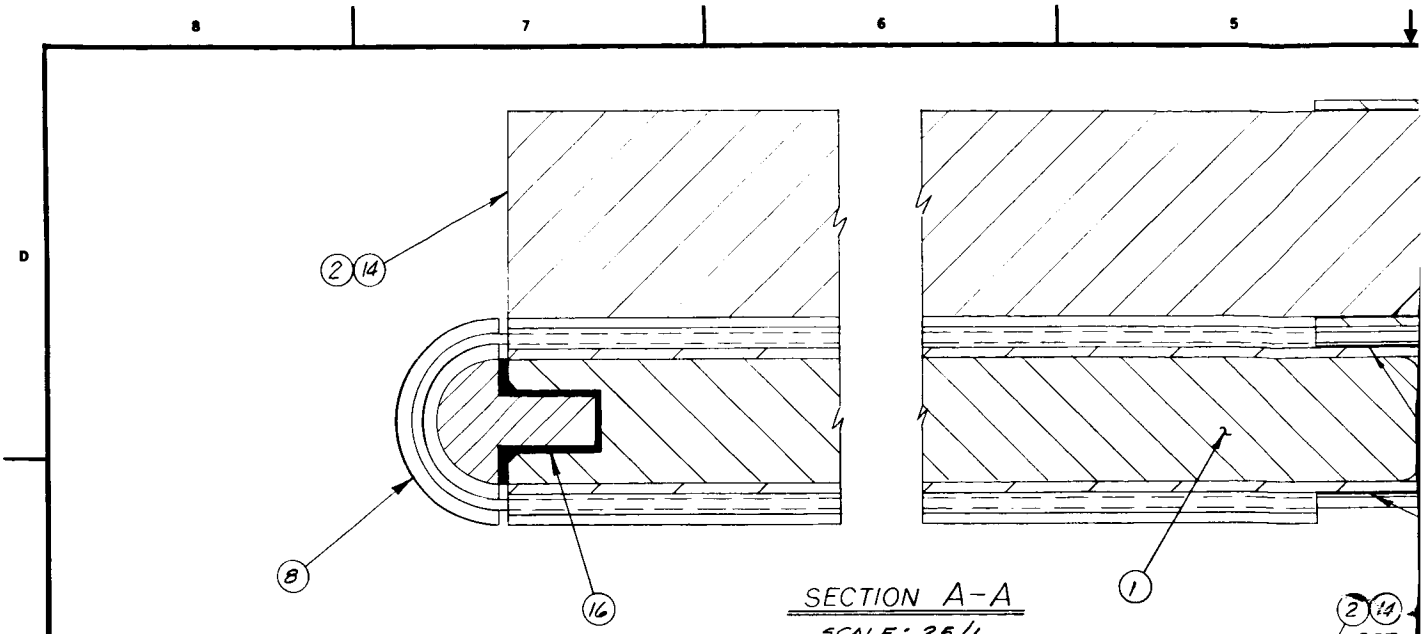
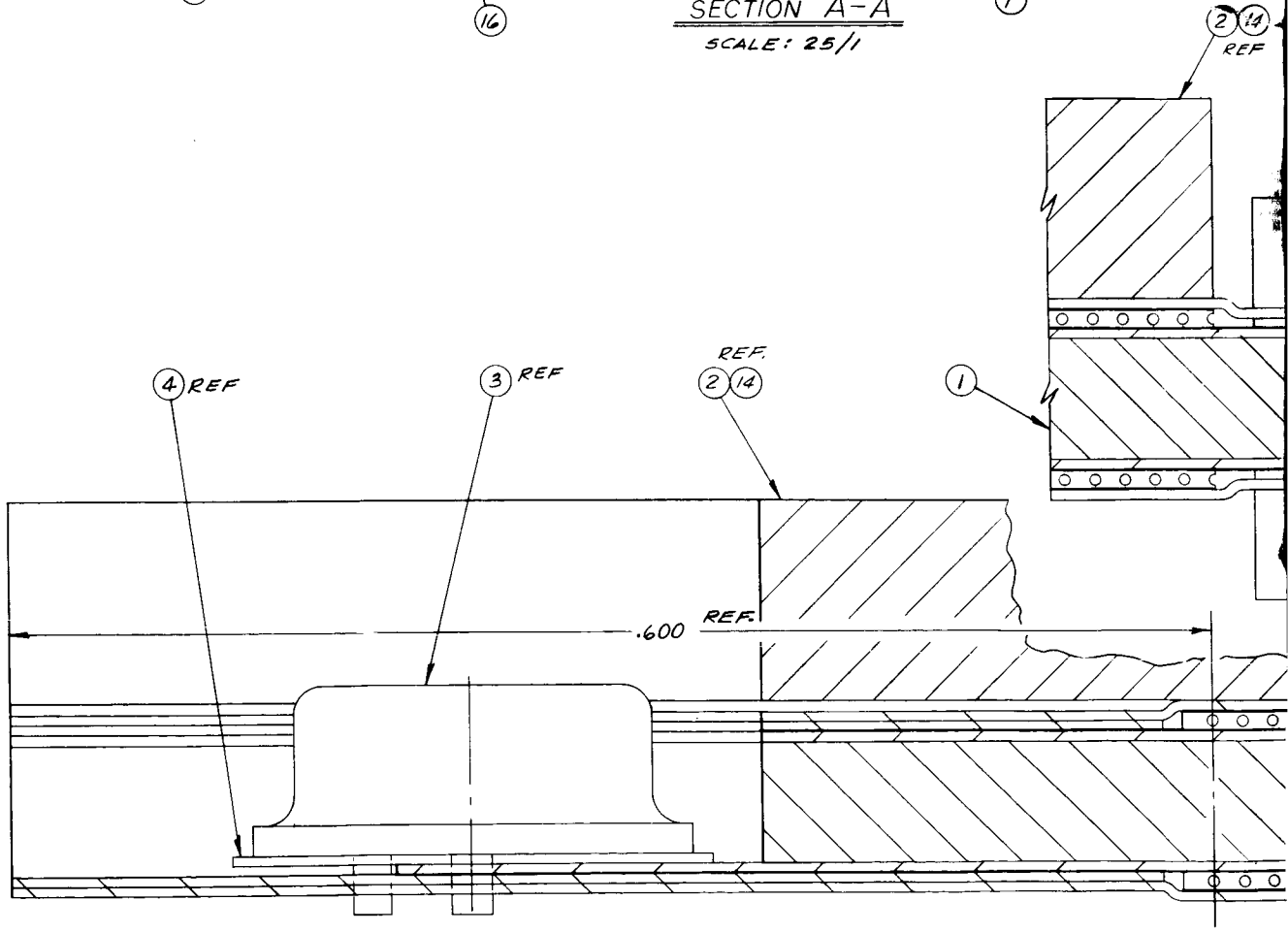


SECTION A-A
SCALE: 25/1



SECTION C-C
SCALE: 25/1

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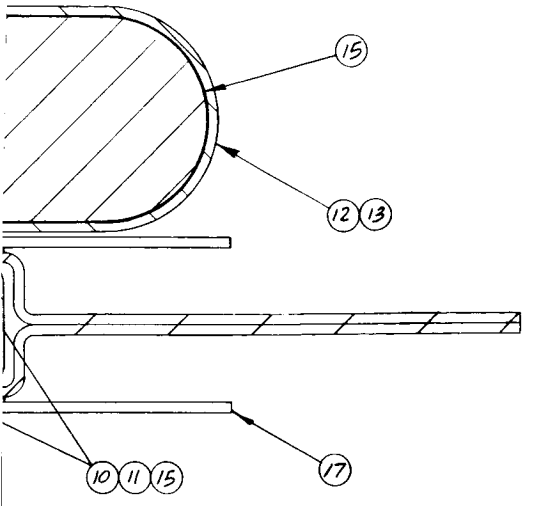
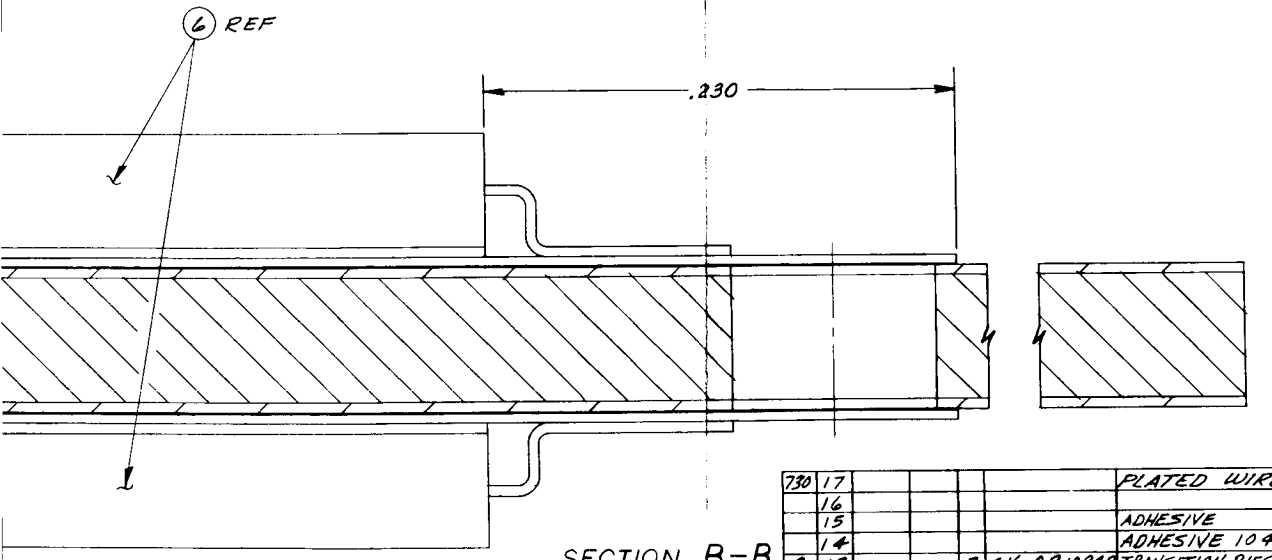
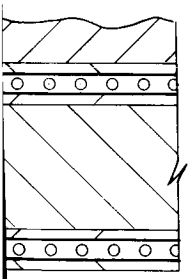
REVISIONS						
SYM	ZONE	ECR	DESCRIPTION	CHK	DATE	APPROVED





SECTION B-B
SCALE: 25/1



QTY REQ'D	FIND	REF DES	CODE IDENT	SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
730	17					PLATED WIRE
	16					
	15					ADHESIVE
	14					ADHESIVE 1044R
2	13			B	SK AP1084-2	TRANSITION PIECE, LONG
2	12			B	SK AP1083-2	TRANSITION PIECE, LONG
2	11			B	SK AP1084-1	TRANSIT. PIECE, SHORT
2	10			B	SK AP1083-1	TRANSIT. PIECE, SHORT
	9					
4	8			B	SK AP1088	COMB - 183 SPACES
	7					
24	6			B	SK AP1037	DIODE
8	5					RESISTOR
2	4			B	SK AP1079	INSULATOR, TRANSISTOR
8	3					TRANSISTOR
1	2			D	SK AP1081	SPACER ASSY
1	1			D	SK AP1086	OVERLAY & FRAME ASSY

LIST OF MATERIAL

PART NO.
IDENT. NO.

NEXT ASSY | EQUIPMENT
APPLICATION
COMMODITY CODE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES TOLERANCE ON
2 PLACE DECIMALS ± /
3 PLACE DECIMALS ± .005
ANGLES ± /
HOLE DIAMETER TOLERANCE
0 THRU .250 +.003 −.002
.251 THRU .500 +.005 −.003
.501 & LARGER +.010 −.005
THREADS: EXT CL 2A, INT CL 2B
MATERIAL
FINISH

LAYOUT G. KAMINSKY 6.24.66
DRAFTSMAN G. Kaminsky 6.28.66
CHECKER
ENGINEER R. HOFFMAN
APPROVAL

CLASS C

UNIVAC
DIVISION OF SPERRY RAND CORPORATION

TITLE PLANE ASSY, Part 2

CODE IDENT NO. | SIZE D | DWG NO. SK AP1087

SCALE 5/1 | WEIGHT | SHEET 2 OF 2

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SECTION 6

NEW TECHNOLOGY REPORT

UNIVAC Research Operations

Blue Bell, Pa.

Under Contract to NASA Goddard Space Flight Center
NAS5-9518

Report No. 1

July 1965

Problem: To provide a means of obtaining the proper information from the memory when a balanced bit-sense matrix is employed.

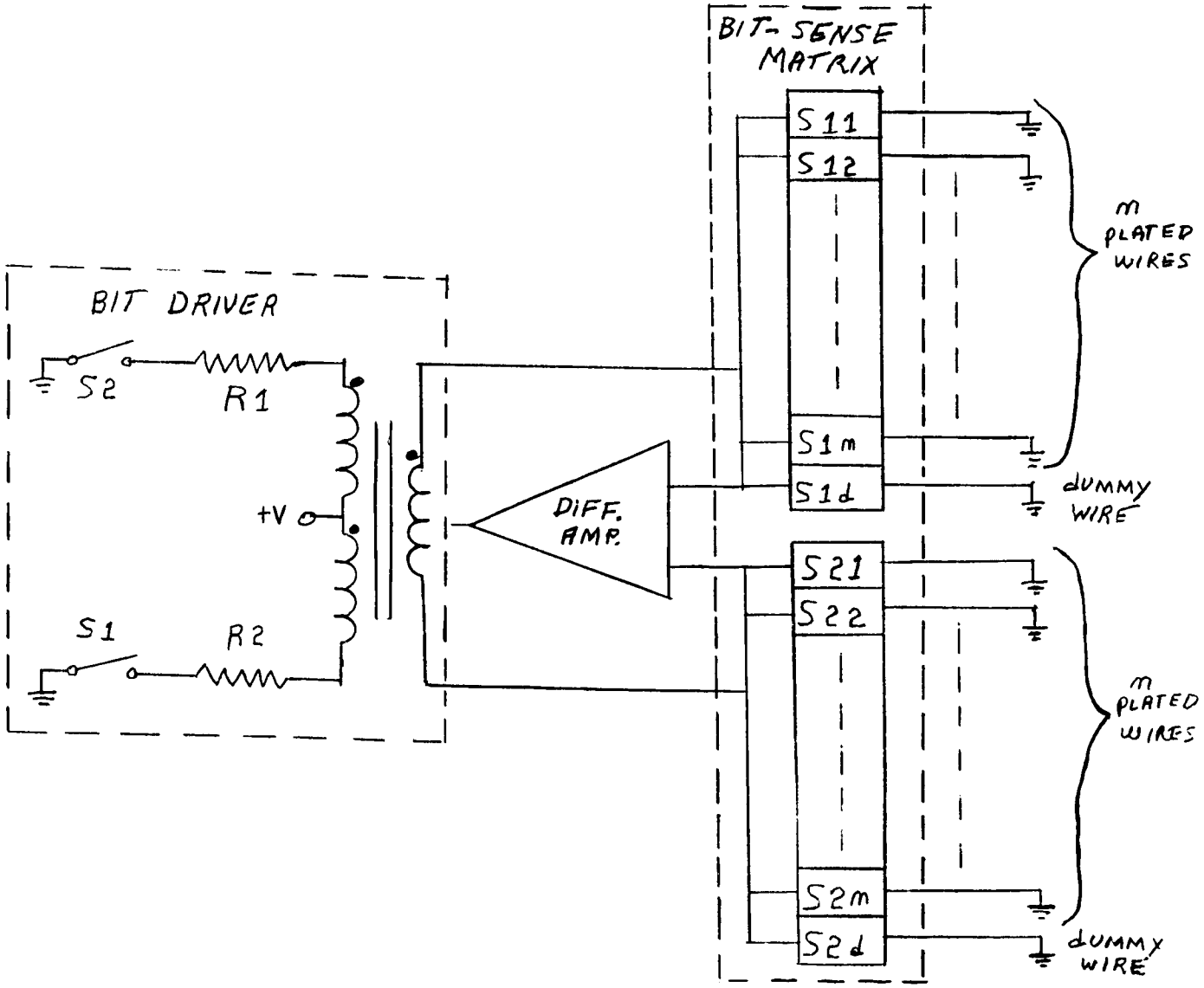
Solution: The polarity of the information is made dependent upon the half of the balanced bit-sense matrix through which the information passes. A transformer is used at the output of the bit driver so that the appropriate polarity reversal of the information is obtained.

How it is done: The bit-sense matrix selects the plated wire from which information is to be read during a read cycle or into which the information is to be written during a write cycle. The bit-sense matrix is comprised of a group of transistor switches. There is one such switch in for every plated wire and dummy wire. Normally, these switches present a high impedance. During a read cycle one of the switches in series with a plated wire is turned on to a low impedance so that the read signal from the plated wire is connected to one side of the differential amplifier which is the first section of the read amplifier. A dummy wire is connected to the other side of the differential amplifier such that rejection of common mode noise is obtained. There is, however, some noise which can couple through the capacitance of the matrix switches which are off. The balanced bit-sense matrix is used to provide cancellation of this noise, the number of switches connected to each side of the differential amplifier, which is the first stage of the read amplifier, being made equal. When a plated wire on one side of the matrix is selected, the dummy wire on the other side is used by turning on its matrix switch.

The problem that arises with the balanced bit-sense matrix is that if the same information is represented by the same polarity of signal on both sides of the balanced matrix, the read amplifier will detect the information differently for the different sides of the matrix. One solution to this problem would be to reverse the information coming from one side of the matrix after it has been detected. The use of the transformer at the output of the bit driver, however, writes the information in such a manner that it will be detected properly such that no additional circuitry is necessary to reverse the information.

How it is done: (Con't)

The polarity of the signal stored in a plated wire is dependent upon the polarity of the bit current. Thus, a positive bit current will write one polarity and a negative bit current will write the opposite polarity. The information to be written is determined by which bit driver transistor switch (S1 or S2) is closed. Closing one of the switches will cause a positive current to flow to one side of the matrix and a negative current to the other because of the transformer action. Therefore, closing one of the switches will write the same information with opposite polarities through the different halves of the matrix and the information will be detected correctly by the read amplifier.



C. A. Nelson

New Technology Report

UNIVAC Research Operations

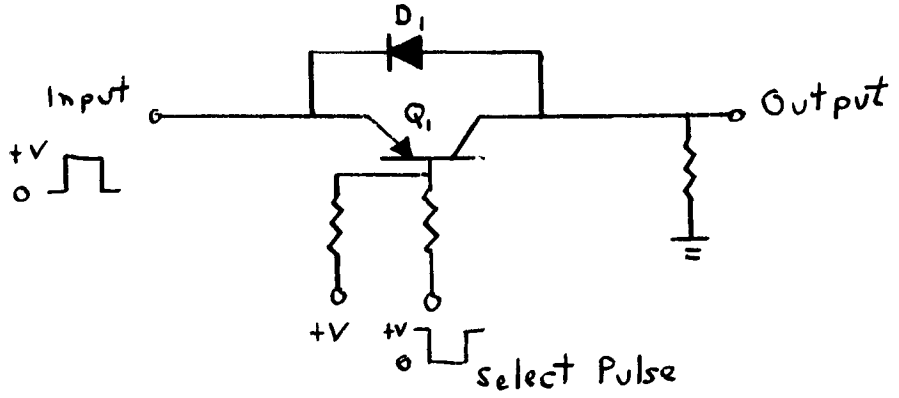
Blue Bell, Pa.

Under contract to NASA Goddard Space Flight Center
NAS5-9518

July 1965

Report No. 2

Diode-Transistor Bidirectional Switch



Problem: To preserve the source impedance of a pulse source as it passes through a solid state switch when the source impedance is much lower than the load impedance.

Solution: An additional path for current flow is provided during the trailing edge of the pulse.

How it is done: During the leading edge and flat top portions of the input pulse Q_1 conducts connecting the output to +V. During the trailing edge of the pulse, D_1 conducts maintaining a low driving impedance for the load allowing a fast fall time. The select pulse permits the input to pass through the switch to the load.

Notes: The circuit is particularly applicable in low power applications.

E. N. Schwartz

jam

New Technology Report

UNIVAC Research Operations

Blue Bell, Pa.

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NAS5-9518

Report No. 3

July 1965

Problem: To enable the use of reed switches for an inexpensive selection scheme in the testing of magnetic elements in spite of the extraneous magnetic fields of the reed switch coils.

Solution: The radiated magnetic field was reduced in two ways by adding a magnetic shield to the reed relay package.

How it is done: Before the reed relay units are packaged, a magnetic shield is inserted which accomplishes two purposes. It attenuates the magnetic field and makes the coil more efficient allowing a reduction in the coil voltage rating.

Notes: In this particular application the external magnetic field was reduced 16 to 1.

E. N. Schwartz

New Technology Report

UNIVAC Research Operations

Blue Bell, Pa.

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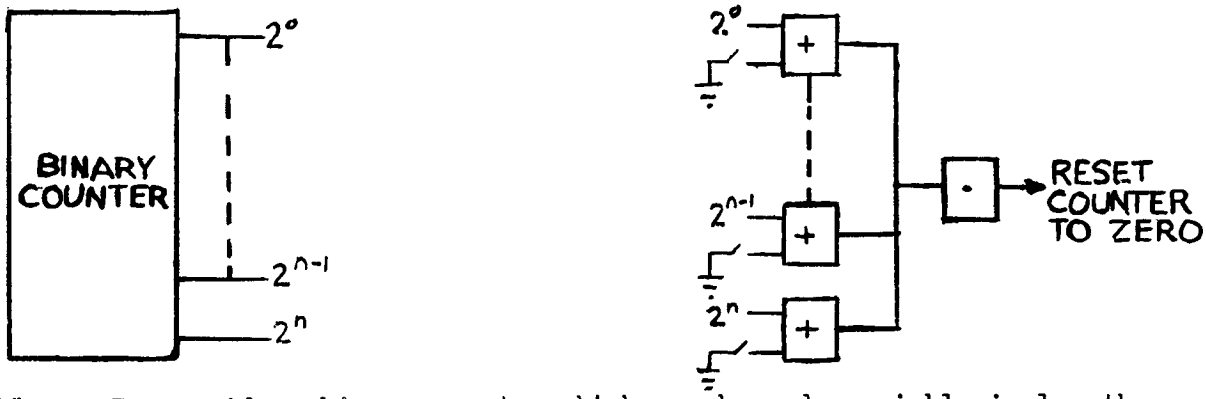
NAS5-9518

Report No. 4

July 1965

Adjustable Counter



Problem: To provide a binary counter which can be made variable in length by means of selector switches.

Solution: A "clear" pulse is generated at a binary count predetermined by a bank of switches. This pulse resets the counter to zero when the counter reaches the last desired count.

How it is done: A gate for each binary output is controlled by means of a switch. The gates are selected by opening the selector switches. When the output of every stage that has been selected is present, a clear pulse is generated resetting the counter to zero.

Notes: The counter will count until the weight of the counter equals the weight of the switches. Thus, for a six stage counter, the counter will count up to a maximum of 63.

E. N. Schwartz

New Technology Report

UNIVAC Research Operations
Blue Bell, Pa.

Under Contract to NASA Goddard Space Flight Center
NAS5-9518

Report No. 5

July 1965

Low Power Ring Counter Drives High Level Loads

Problem: To design a ring counter which dissipates very low power in standby conditions, yet can drive high-current loads on a low duty-factor basis.

Solution: A counter was designed using complementary transistors so that in the one selected stage, both transistors are conducting, while the transistors of the other stages are all cut off. The two transistors in the selected stage carry a very low holding current, so that the standby dissipation is small. When high level drive capabilities are required, the holding current is augmented by a pulse of higher current without changing the state of the counter.

How it is done: In a counter stage, transistors Q_1 and Q_2 form a variation of a silicon controlled switch. Once the pair has been turned on by a pulse of current into the base of Q_2, they will remain saturated as long as current is flowing through the emitter of Q_1. When this holding current is removed, both transistors turn off. While a stage is on, the amplitude of this holding current may be varied over a very wide range without changing the state of the transistors.

A ring counter is made of a number of stages interconnected as shown. By capacitively coupling the output of one stage to the input of the next, the positive-going wavefront of a stage turning off serves to turn on the following one. Counter operation is initiated by pulsing the Reset circuit. This turns on the first stage and turns off any other which might be on. Holding current then flows through R_1 and the Common Anode Line into the first stage. The counter is stepped by momentarily turning on Q_3, thus shunting the holding current. This causes the first stage to turn off and the second to turn on.

Two types of high current loads may be driven from the counter stage. The first, connected to Output 1, accepts current. The second, connected to Output 2, supplies current. Drive capability for both types is provided by pulsing the High Level Drive circuit. This supplements the holding current to the extent required by the load. Since this high level capability is required for very short times, the average dissipation is low.

New Technology Report No. 5
UNIVAC Research Operations
July 1965

Note: A ring counter requires one stage per count, in contrast to a binary counter in which n stages provide a count of 2^n. In order to cut down on the number of ring counter stages required to achieve a high count, it is possible to use two-dimensional matrix selection. In this technique, two ring counters are used with the product of the numbers of their stages equalling the required count. The counters are arranged so that each time one counter steps through all its stages, the second counter is stepped once. Thus, by the time the second counter has stepped through all of its stages, the number of distinct combination achieved is equal to the product of the counters' stages.

R. Mosenkis

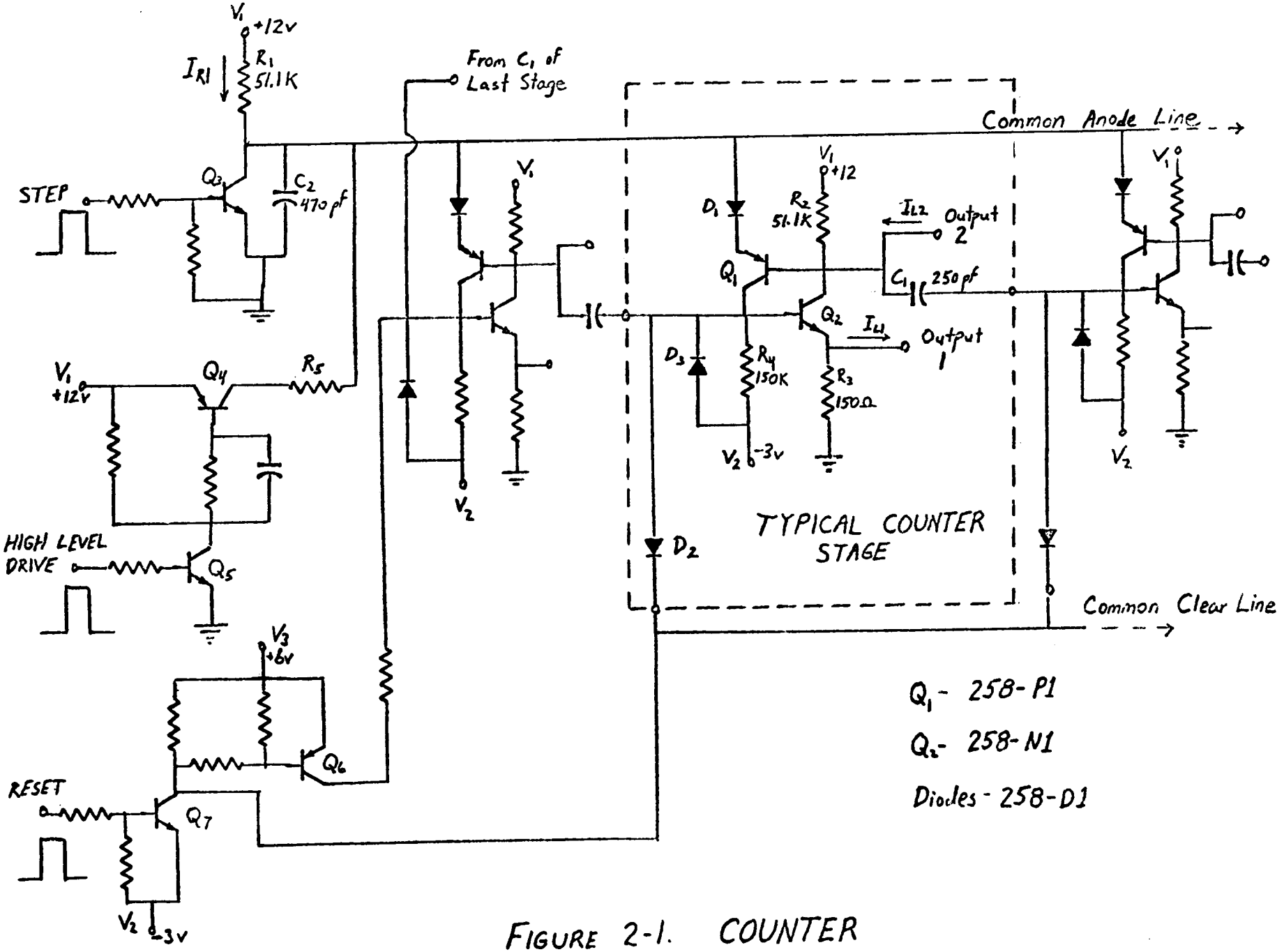


FIGURE 2-1. COUNTER

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NAS5-9518

Report No. 6

July 1965

NDRO Memory Word Current Regulation Eased

Problem: To ease the task of regulating the word current in a non-destructive readout film memory without sacrificing readout signal amplitude.

Solution: Generate a word current pulse with a slow leading edge and fast trailing edge. Read (sense) on the trailing edge.

How it is done: Since the word drive line is inductive, the rise time of the word current can be controlled by limiting the voltage from which the current is driven. Slowing the rise time will eliminate over shoot and ringing problems which add to the word current tolerance.

Notes:

1. By using a lower supply voltage to drive the word current, power dissipation is reduced.

2. The full time of the word current can be made fast, so that readout amplitude is not sacrificed. When reading on the leading edge of the word current pulse, the sensed signal amplitude is strongly dependent on the waveshape of the last portion of the rise. Due to the reactive nature of the word lines, it is difficult to control this portion. On the other hand, when sensing on the trailing edge, the initial portion of the fall of word current is significant in determining the output signal amplitude. This is also the easier portion of the fall to control.

R. Mosenkis

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UNIVAC Research Operations

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NAS5-9518

Report No. 7

July 1965

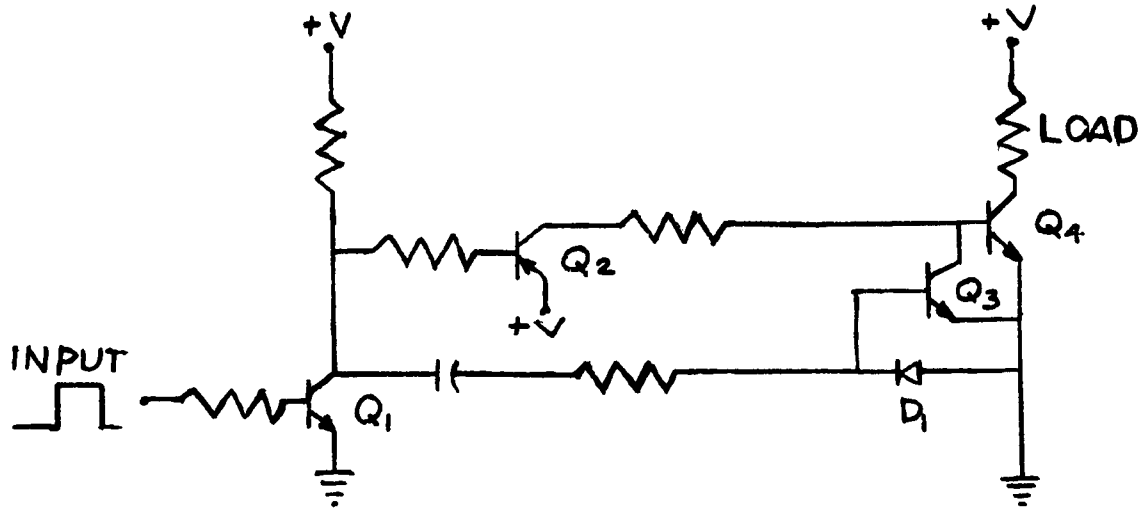
Low-Storage Transistor Switch

Problem: To limit storage time in a high-current saturating transistor switch.

Solution: Use another transistor to clean up the excess base current in the switch.

How it is done: Transistor Q_3 does not affect circuit operation until Q_1 is turned off. When the potential at the collector of Q_1 rises, it turns Q_2 off and Q_3 on. Since the collector saturation voltage of Q_3 is much lower than the base saturation voltage of Q_4, excess base current is drawn out of Q_4, thus lowering its storage time.

Notes:
1. This technique provides a lower impedance cleanup path than would resistor to a reverse bias. It is useful where Q_4 must be driven into saturation either because its dissipation out of saturation would be excessive or because a tightly-controlled voltage must be applied across the load.
2. The circuit uses no standby power, making it useful in aerospace application. It may be used in a single-supply system.



R. Mosenkis

New Technology Report

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Blue Bell, Pa.

Under contract to NASA Goddard Space Flight Center
NAS5-9518

Report No. 8

July 1965

Problem: To obtain a gated section of amplification in which the ratio of the gain when the gate is on to the gain when the gate is off is very large and in which the noise produced by the gate is very small as compared to the signal amplitude.

Solution: The section of amplification is comprised of two transistor stages with very large negative feedback from the second stage to the first. When the gate signal is applied the negative feedback is eliminated, and the gain of the section of amplification becomes the product of the gain of the two common emitter stages.

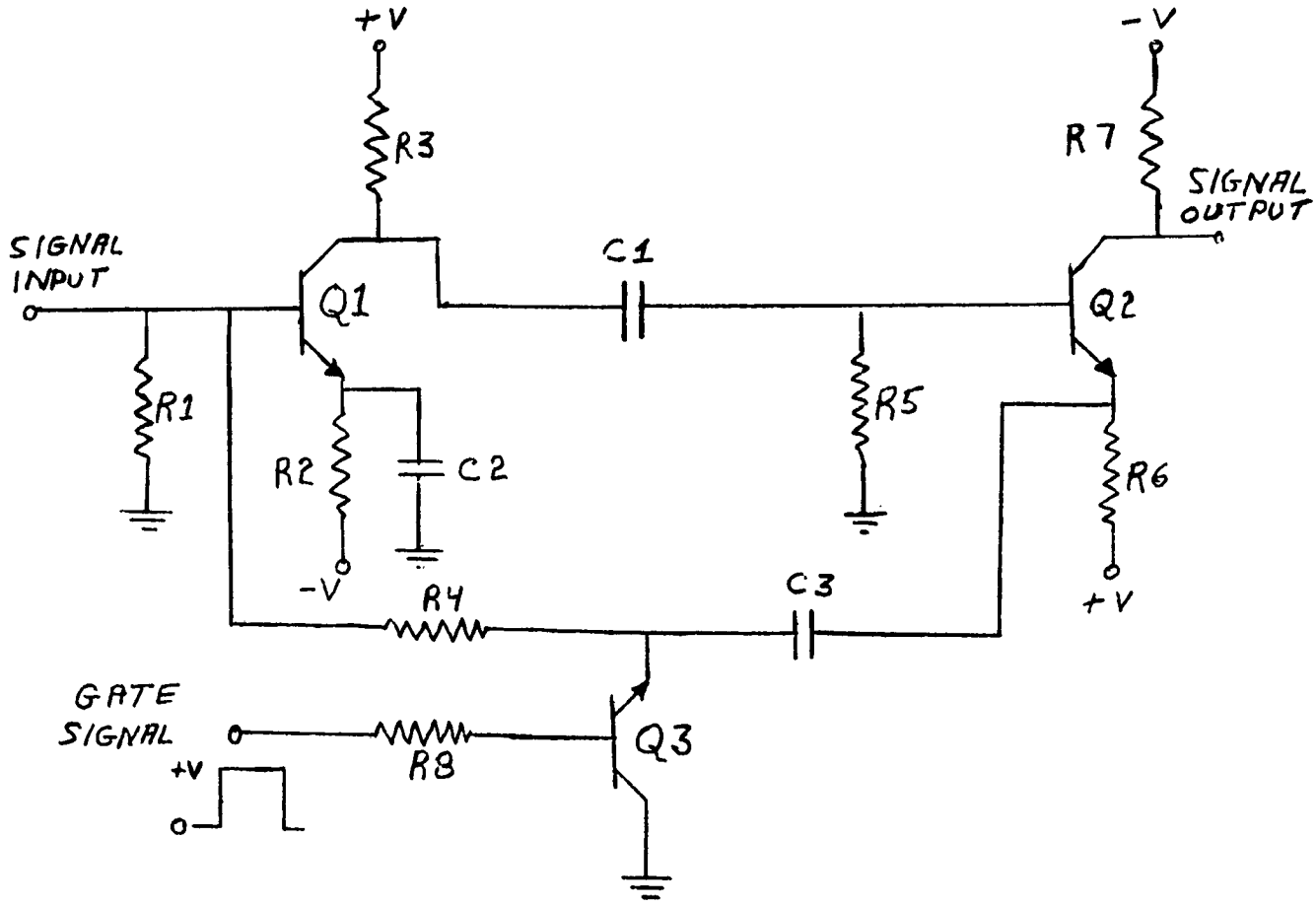
How it is done: Transistors Q_1 and Q_2 are biased in the linear region, the bias currents being determined by resistors R2 and R6. Q_3 is the transistor which performs the gating function. When the gate signal is not applied Q_3 is off and presents a very high impedance, and the gain of the section of amplification is made very small by the large negative feedback from the emitter of Q_2 to the base of Q_1. The negative feedback is made large by making the feedback resistor R4 an order of magnitude smaller than R6.

When the gate signal is applied, transistor Q_3 presents a low impedance at the emitter of Q_2. The two stage negative feedback is essentially eliminated by making the saturation resistance of Q_3 an order of magnitude smaller than the feedback resistor R4. The gain of the section of amplification thereby becomes the product of the gains of the two common emitter stages. Capacitors C2 and C3 are made large enough to act as signal bypass capacitors.

The noise generated by the gate transistor Q_7 is the emitter offset voltage of approximately 2 mv. This is small as compared to the signals being amplified so that effective gating is employed.

New Technology Report No. 8 (Con't)
UNIVAC Research Operations
July 1965

Notes: The circuit is used as part of a memory read amplifier. A positive signal at the base of Q_1 is to be amplified. Low transistor bias currents of 50 ua are employed to provide low power amplification. Complementary stages of amplification allow large signal outputs. Low gain is necessary when the gate is off to allow recovery at the low power level from transients that occur at the beginning of the memory cycle. The noise generated by the gate is of the polarity to aid the signal amplification.



C A Nelson

C. A. Nelson

New Technology Report

UNIVAC Research Operations

Blue Bell, Pa.

Under contract to NASA Goddard Space Flight Center
NAS5-9518
Report No. 9
July 1965

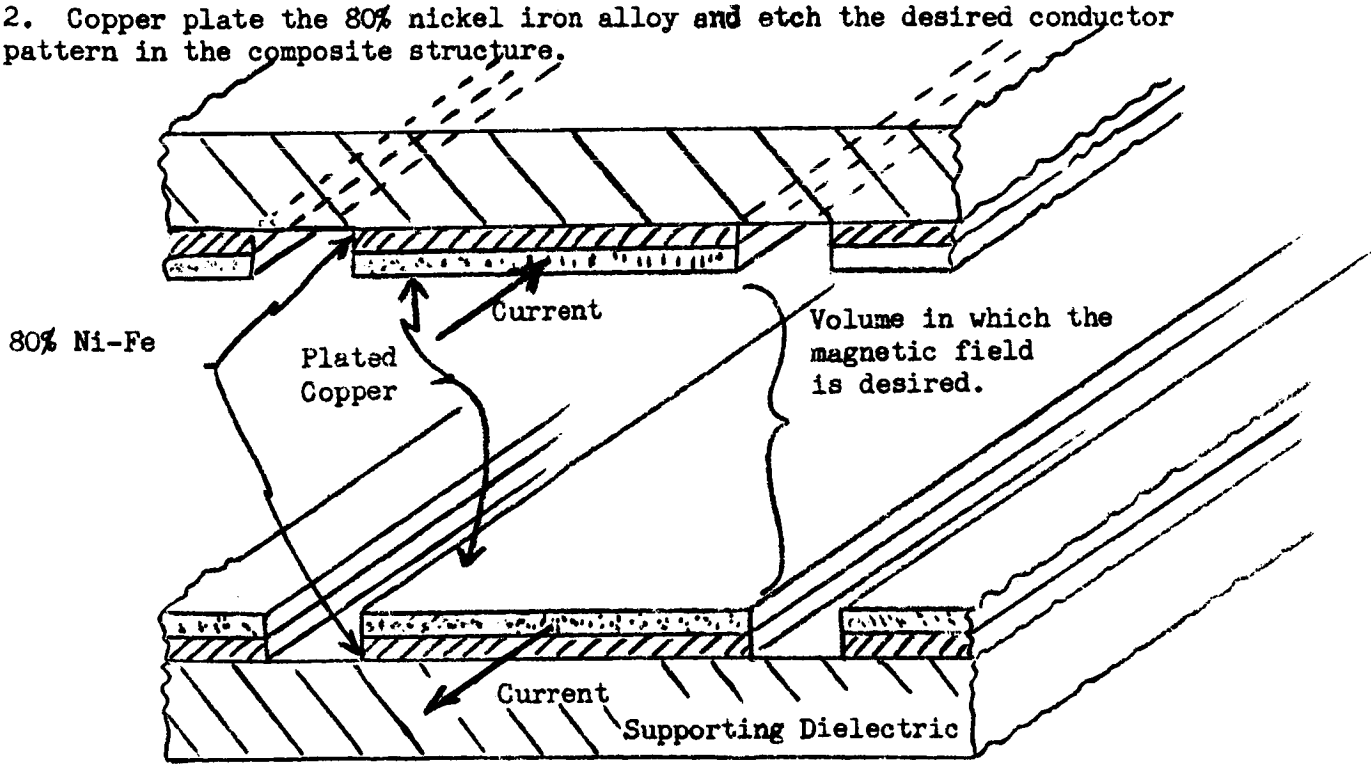
Problem: Produce a pulse magnetic field within the interior of a strip transmission line. The magnetic field intensity has a fixed amplitude and must have a very short, approximately 35 x 10^{-9} sec., rise and fall time and a duration of 0.3 to 0.4 microseconds. The current required to produce this magnetic field must be kept as small as possible.

Solution: The strip transmission line is etched copper conductor pairs or a single line over a ground plane. Use of a 80% nickel iron alloy in addition to the copper lines will reduce the required current nearly 50%.

How it is done:

1. Laminate the 80% nickel iron alloy to the supporting dielectric. Trade mark names of appropriate alloys are Shield-mu 30, Conetic AA, Mumetal, HyMu "80", and others.

2. Copper plate the 80% nickel iron alloy and etch the desired conductor pattern in the composite structure.



Cross Section of Strip Transmission Line

Notes: The 80% nickel-iron alloy is bonded to Kapton* film with an adhesive film. The adhesive film is type FM1041R from Bloomingdale Rubber Co., Havre de Grace, Md. The lamination is done at 650 p.s.i., 350°F for one hour. The surface of the 80% nickel iron alloy is prepared by detergent cleaning and rinse, etched in ferrichloride, dipped in 25% hydrochloric acid and rinsed and dried. Approximately 0.0001 to 0.0002 inches of material is removed by the etching step.

The copper is plated in a common cyanide bath. Etching of the final conductor pattern is done with Kodak KPR photo resist and ferric chloride etchant.

*E. I. DuPont Trademark, Kapton Polyimide Film Type H.

G. A. Fedde

APPENDIX I

DETAILED DESCRIPTIONS OF ALL CIRCUITS DESIGNED FOR THE MINIATURE SPACEBORNE MEMORY

TECHNICAL REPORT NO. 71

TITLE: Logic and Control Circuits

ENGINEER: E. N. Schwartz

PROJECT: 258

CONTRACT: NAS 5-9518

DATE: August 5, 1965

ABSTRACT:

This report contains a description of the logic and control circuits which are used in the memory timing chain and in the parallel to serial converter. The design of the information register is also included.

Written by: _____
E. N. Schwartz

Approved by: _____
G. A. Fedde

jam

TECHNICAL REPORT NO. 71

A. DELAY FLOP - (Monostable Multivibrator, DF)

1. Specifications

a) Triggers on positive wavefront at point C. Wavefront must have a risetime less than 100 nanoseconds and must have a positive excursion greater than 2 volts.

b) Input current required - 4 milliamps.

c) Positive output pulse from point A (0 to +6) can supply 8.5 milliamps.

d) Positive going edge at conclusion of output at point E is used to trigger next delay flop in a chain.

e) Point B is used to discharge point A of preceding delay flop in a chain.

f) Circuit operates between +4 and +8 volts between -20°C and +85°C.

2. Output wave forms and connections for timing chain

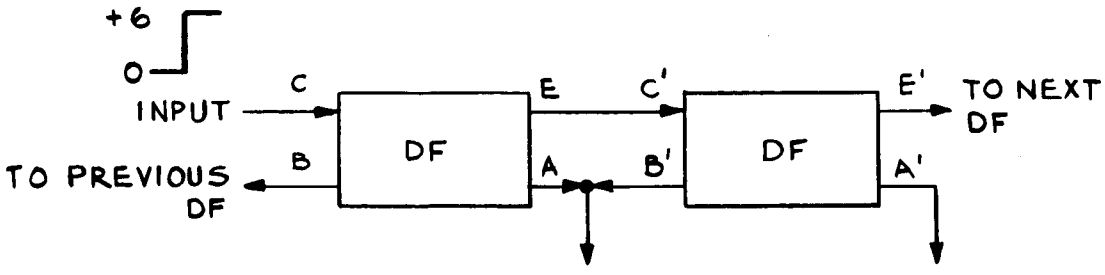


Figure 1

E. N. Schwartz
Whitpain
August 5, 1965

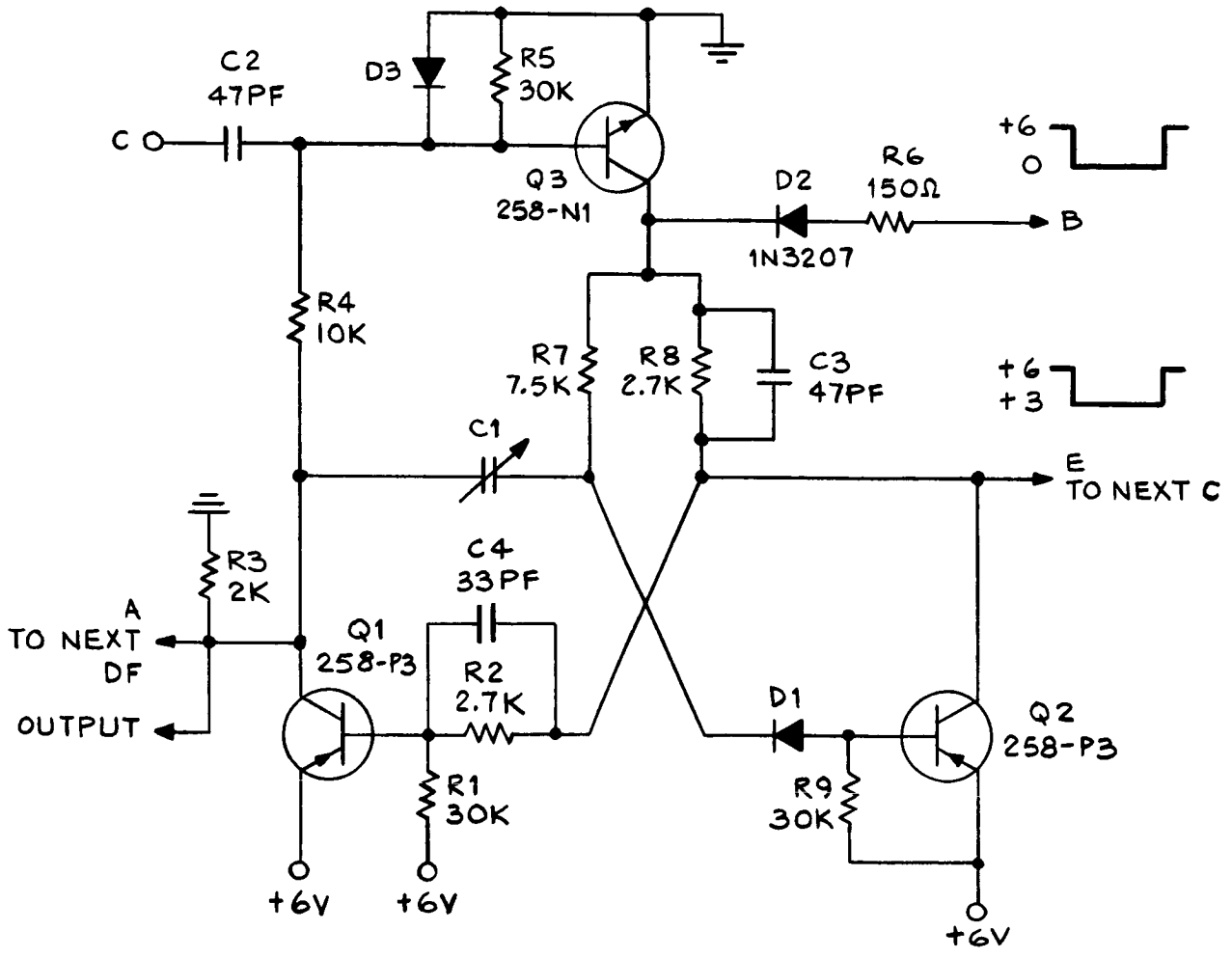


Figure 2

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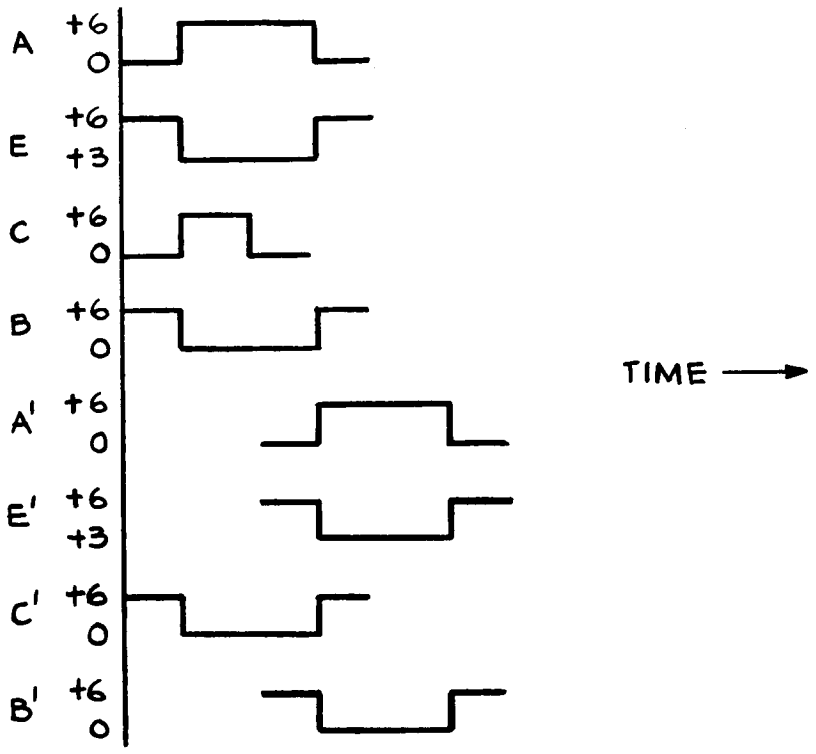

Figure 3

Description

Q1 thru Q3 are all normally off. A positive input at Point C causes Q3 to conduct. Q1 then turns on with its base current supplied thru R8, C3, R2, C4. Q1 will remain on until C1 is charged sufficiently thru R7 to cause Q2 to conduct. While Q1 is conducting, Point E is at approximately +3 volts. When Q2 conducts Q1 turns off since its base current is diverted thru Q2. Q1 was latching Q3 thru R4 and when Q1 turns off Q3 goes off. When Q2 began to conduct Point E went from +3 to +6 and this positive transition can feed the next delay flop.

B. BUFFER REGISTER (BR)

1. Specifications

a) A positive pulse applied to R9 which is greater than +10 volts and longer than 100 nanoseconds will cause Q1 and Q3 to conduct and Q2 and Q4 to turn off provided the input to D3 is greater than +3 volts. The current source supplied from D6 located in the Information Register and applied to the anode of D1 in the Buffer Register will cause Q1 and Q3 to conduct and Q2 and Q4 to turn off provided the input current is applied for 200 nanoseconds.

E. N. Schwartz
Whitpain
August 5, 1965

b) Pulsing the cathode of D4 to ground for 100 nanoseconds will turn on Q2 and Q4 and turn off Q1 and Q3.

c) The register will operate from +4 to +8 volts between -20°C and +85°C.

d) Input to R9 is 3/4 milliamp.

e) Output at D5 can supply 1.7 milliamp.

2. Description

The buffer register is a flip-flop consisting of two complementary pairs connected back to back. This results in a high speed to power ratio speed up capacitors C1 thru C4 help keep the set and reset time low.

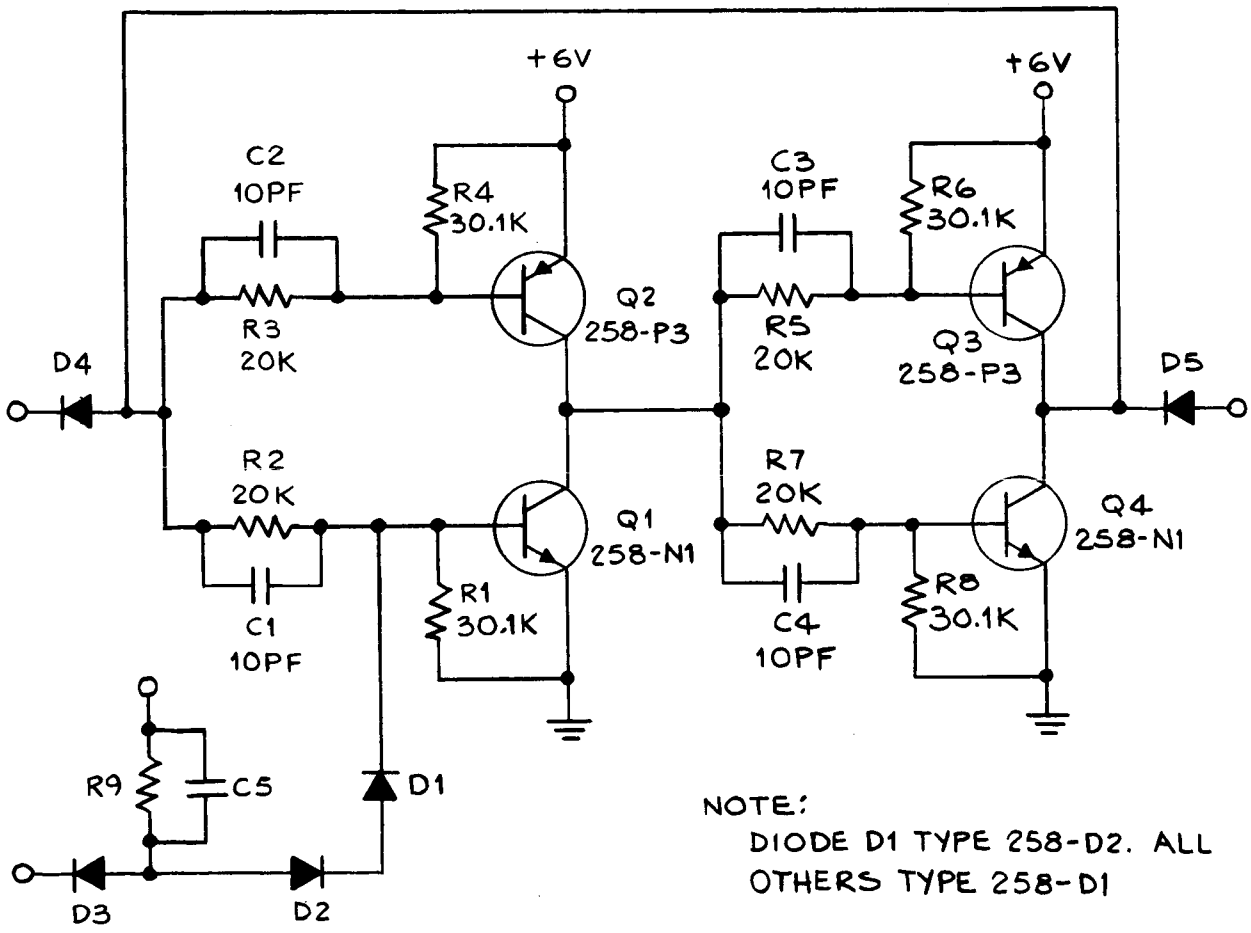

Figure 4.

E. N. Schwartz
Whitpain
August 5, 1965

C. LOW POWER RING COUNTER

1. Specifications

a) Counter advanced once for each input step pulse greater than 100 nanoseconds and less than 500 nanoseconds in width at a rate of up to 2 megacycles. Required stepping rate is 500 K c.p.s.

b) Voltage requirements: must operate at +12 V $\pm$4% and will operate between +5 V and +16 V.

c) Recovery from step pulse: 50 nanoseconds

d) Power dissipation from +12 volts:

4 stage counter	standby 10.8 mw,	500 KC	34 mw
10 stage counter	standby 25 mw,	125 KC	35 mw

e) Output: Each stage supplies complementary outputs with a drive capability of 1 ma.

f) Capacitive loading. Each output can drive 50 pf without significantly affecting performance.

g) Above requirements are met between -20°C and +85°C.

2. Description. One stage of the counter is shown in Figure 5. The stepping circuit provides the optimum amount of energy to the counter provided that the input to the stepping circuit is greater than 100 nanoseconds. This makes the counter operation independent of the width of the stepping pulse.

A high speed-to-power ratio is obtained by using complementary transistor pairs in place of the conventional collector resistor. Each counter stage consists of complementary inverters connected back to back. The emitters of the PNP transistors have a common path to +12 V thru a 150 ohm resistor. Thi resistor improves the stability of the counter.

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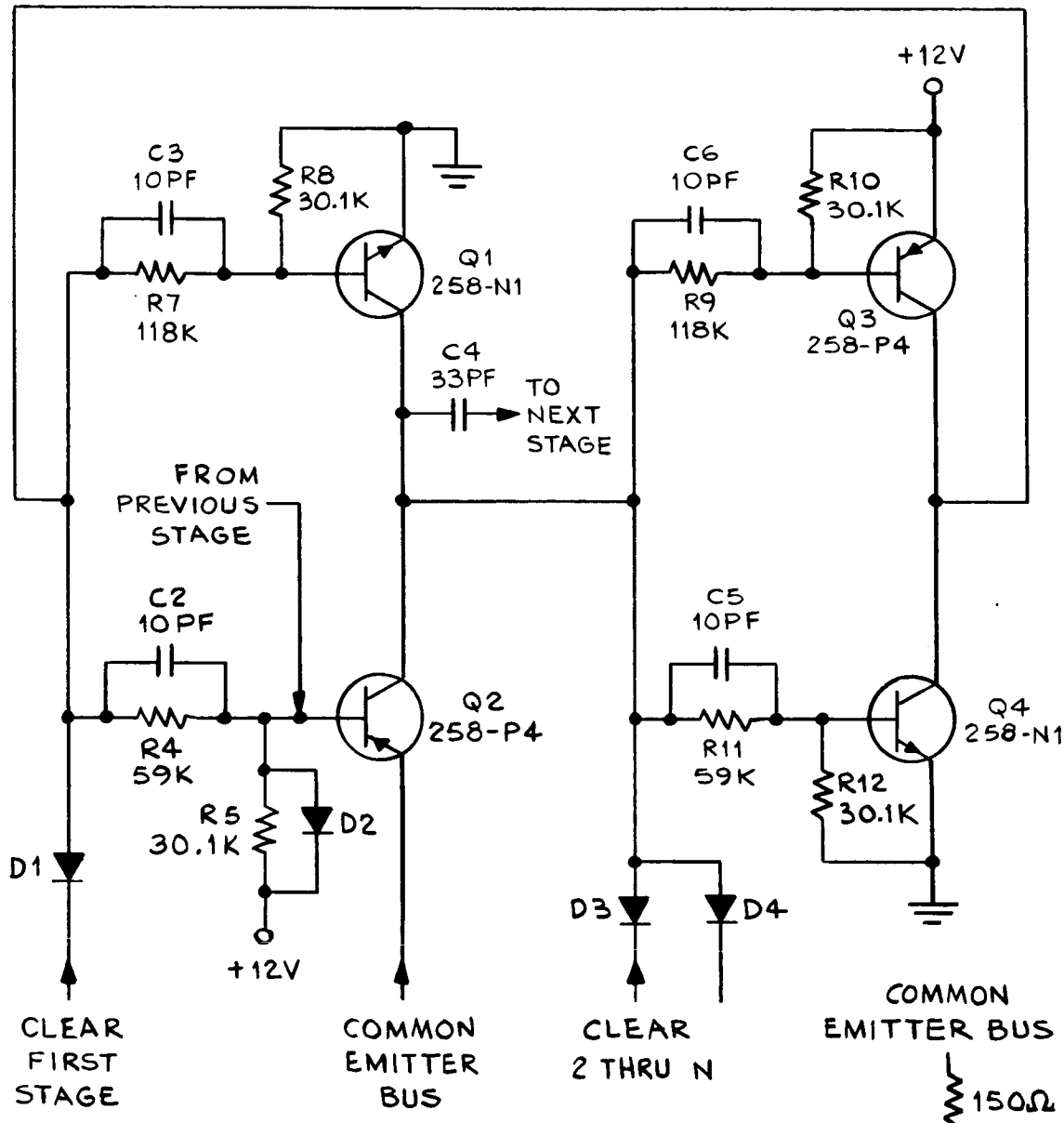
August 5, 1965



NOTE:
DIODES, D1, 2, 3 AND 4 ARE TYPE 258-D1

Figure 5

E. N. Schwartz
Whitpain
August 5, 1965

During normal operation, N stages are connected in a ring. Before counting begins a clear pulse is applied to diode D1 of the first stage and diode D3 of stages 2 thru N. This turns on the first stage and turns off stages 2 thru N. The clear pulse has an off level of +12 V and pulses to ground as does the step pulse. The step pulse is applied to diode D4. When the step pulse is applied, the stage that is on, (Q2 and Q4 conducting, Q1 and Q3 off) is turned off since the step pulse robs base current from Q4 and supplies base current to Q3. The turn off of Q4 and turn on of Q3 causes the turn off of Q2 and the turn on of Q1. The turn on of Q1 is coupled thru C4 to Q2 of the next counter stage causing the next stage to turn on. The on stage will progress around the ring one stage for every applied step pulse.

D. MISCELLANEOUS CIRCUITS

1. Counter Inverter (CINV)

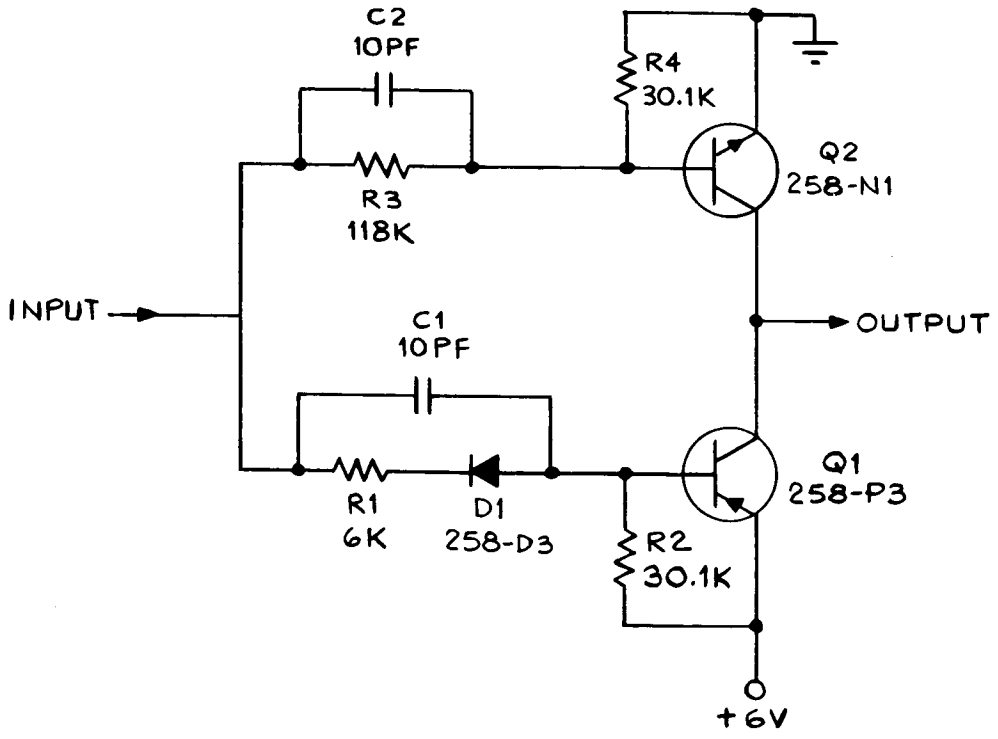


Figure 6

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The circuit is an inverter consisting of a complementary pair. When the input is at zero volts, the output is at +6 V and when the input is at +12 V, the output is at zero volts. Output can supply 6 ma at +6 volts and an input at ground must supply .65 ma.

2. Counter Pulser (CP)

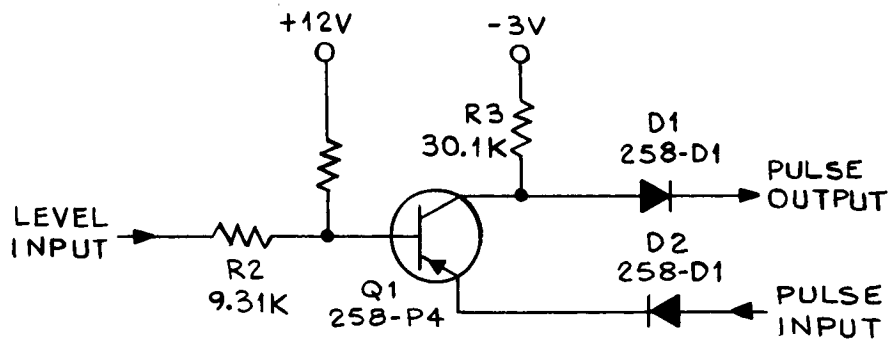

Figure 7

When the level input is at zero volts, a pulse input pulsing to +12 volts w'll cause the output to swing to +12 volts. When the input level is at +12 volts, no output will appear.

3. Pulse Amplifier (PA)

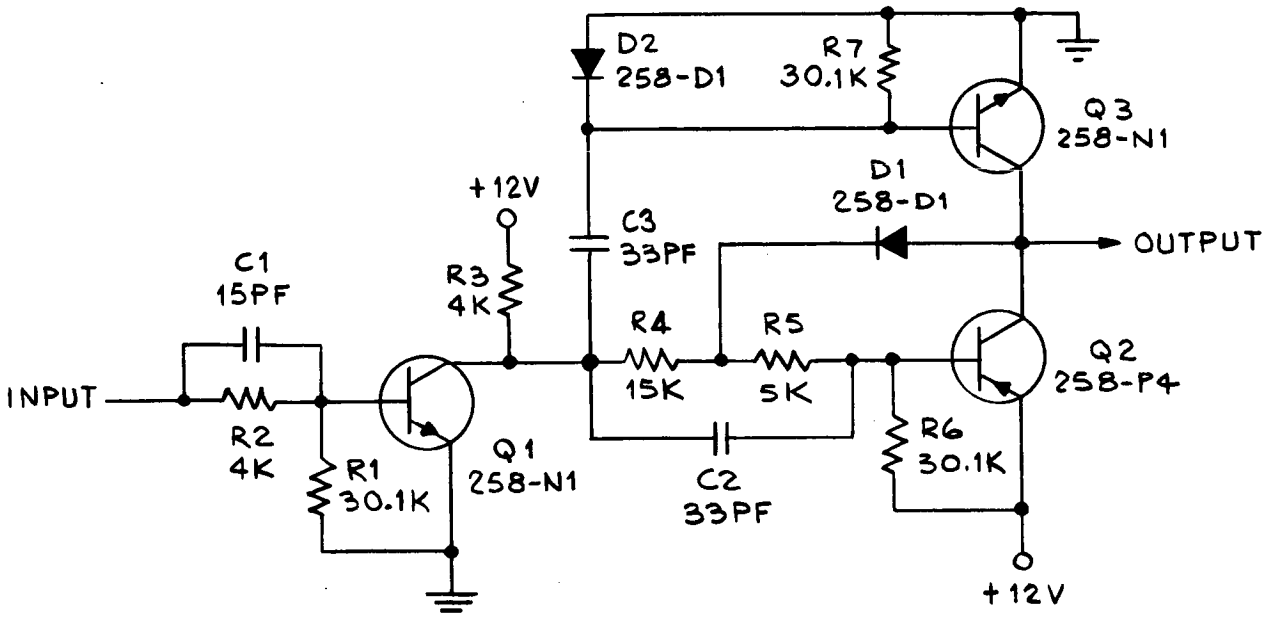

Figure 8

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The function of the circuit is to convert a pulse which swings between 0 and +6 V to a pulse which swings between 0 and +12 volts. The circuit is non-inverting.

4. Pulse Gate (PG)

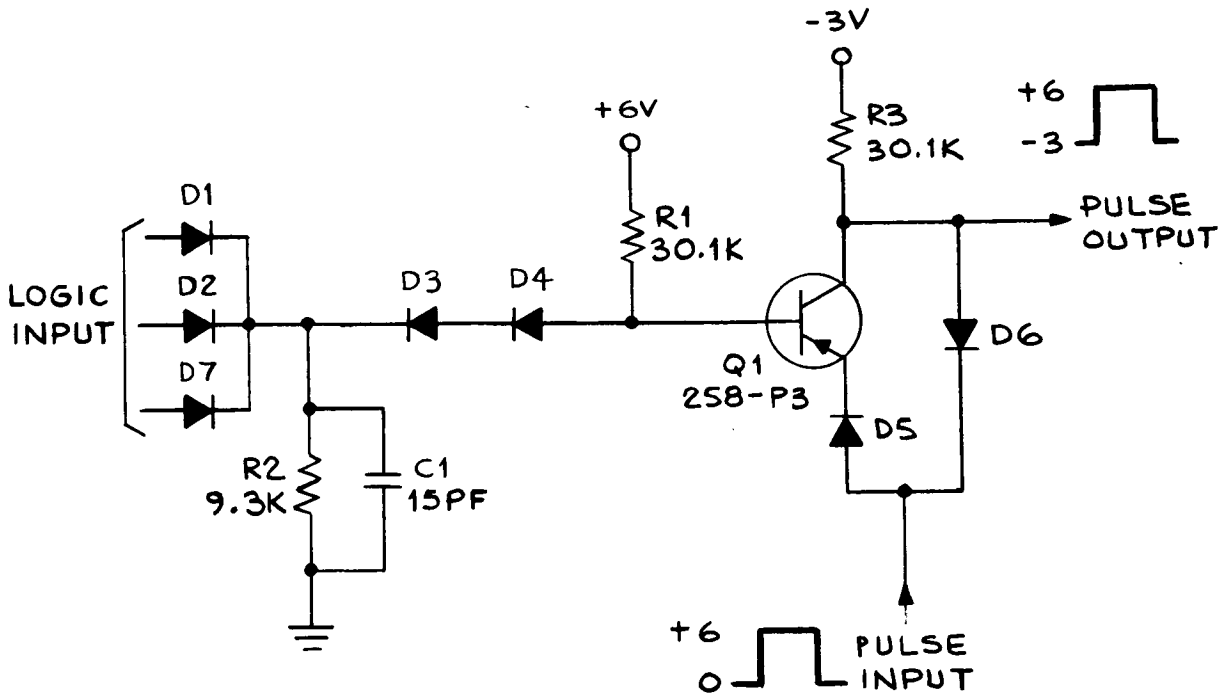

Figure 9

The purpose of this circuit is to allow an input pulse at diode D5 to pass thru Q1 to the output when all logic inputs are at zero volts. Any input at +6 volts will hold off Q1 and prevent the output from pulsing. The purpose of D6 is to cause the output to follow the input during the negative going edge of the input. Logic input must supply 0.6 ma. Pulse input drive required is 1 ma plus load. Output can supply up to 10 ma load.

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5. Information Counter Stepper (CS) and Buffer Reg. Reset (RP)

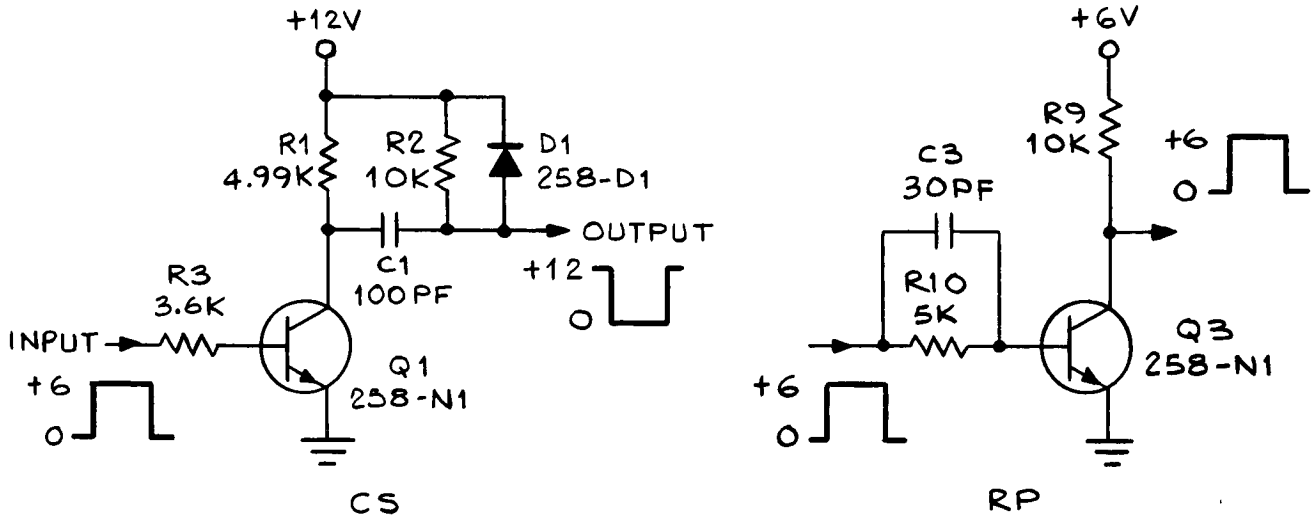

Figure 10

These circuits are used to invert positive going pulses. The CS circuit will deliver a constant amount of energy to the counter regardless of the input pulse width provided the input is wider than 100 nanoseconds.

6. Output Buffer

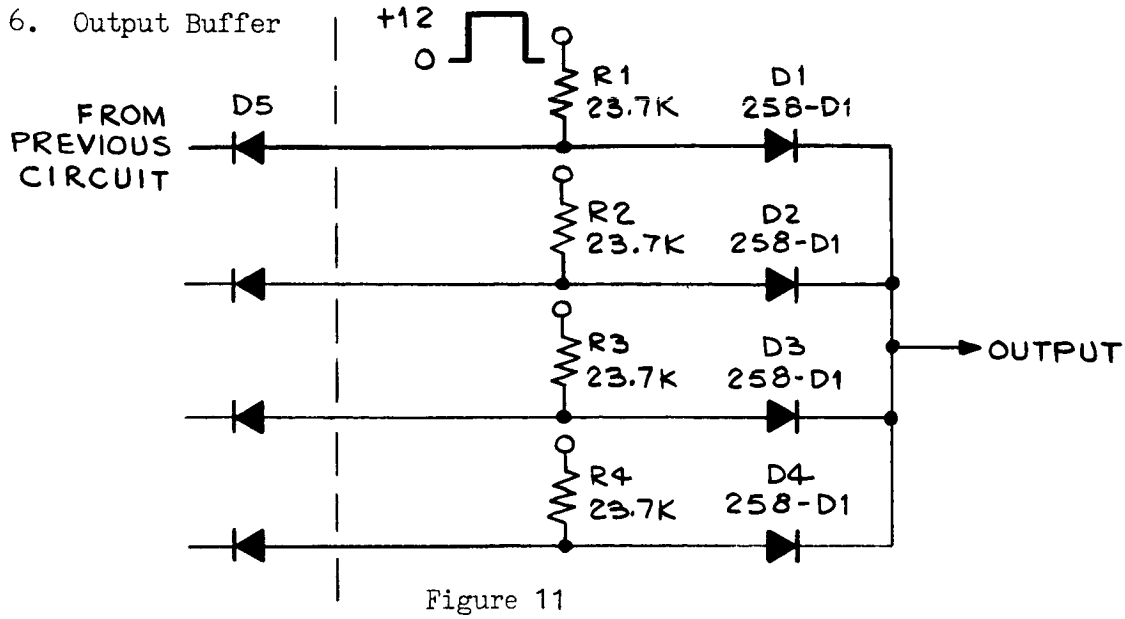

Figure 11

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The circuit consists of four diode resistor gates. When R1 is pulsed from 0 to +12 V, current will flow to the output if the input to D5 is at +6. The current will be drawn away thru D5 if the input to D5 is at zero volts. The current supplied to the gate from the pulse source is 0.5 ma.

7. Logic Inverter (INVI)

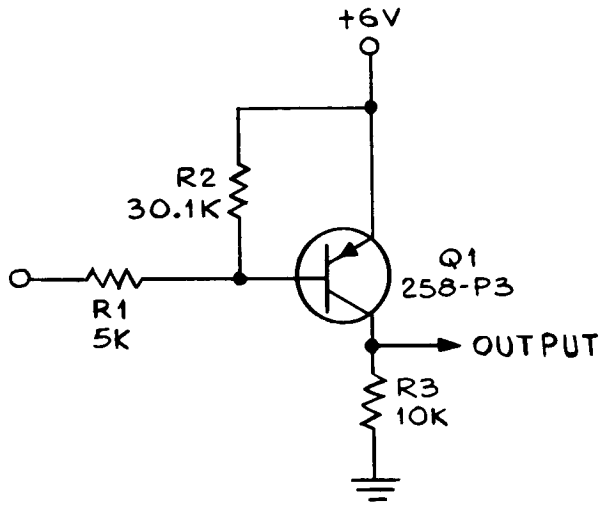

Figure 12

This circuit is used to invert and amplify a level. It can drive 6 ma and requires 1 ma at the input.

8. Logic Gate (GI)

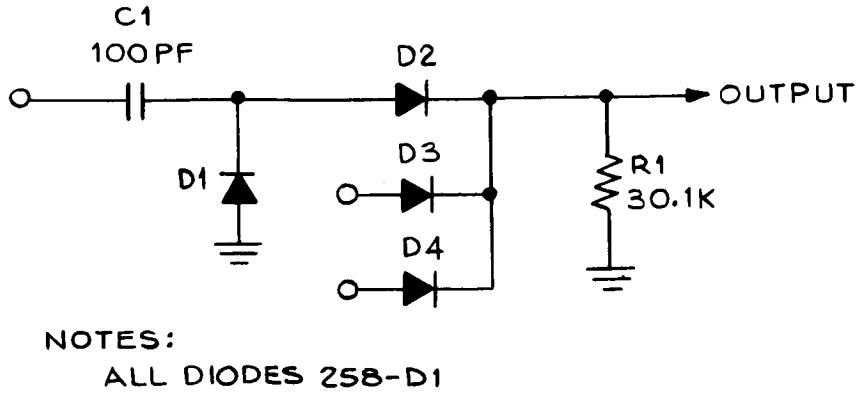

Figure 13

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This circuit is an "or" gate used to trigger a delay flop from a positive going wavefront. The input to C1 is a.c. coupled since a delay flop feeds this point and cannot stand a d.c. load.

9. Information Register (IR) P-HC-04

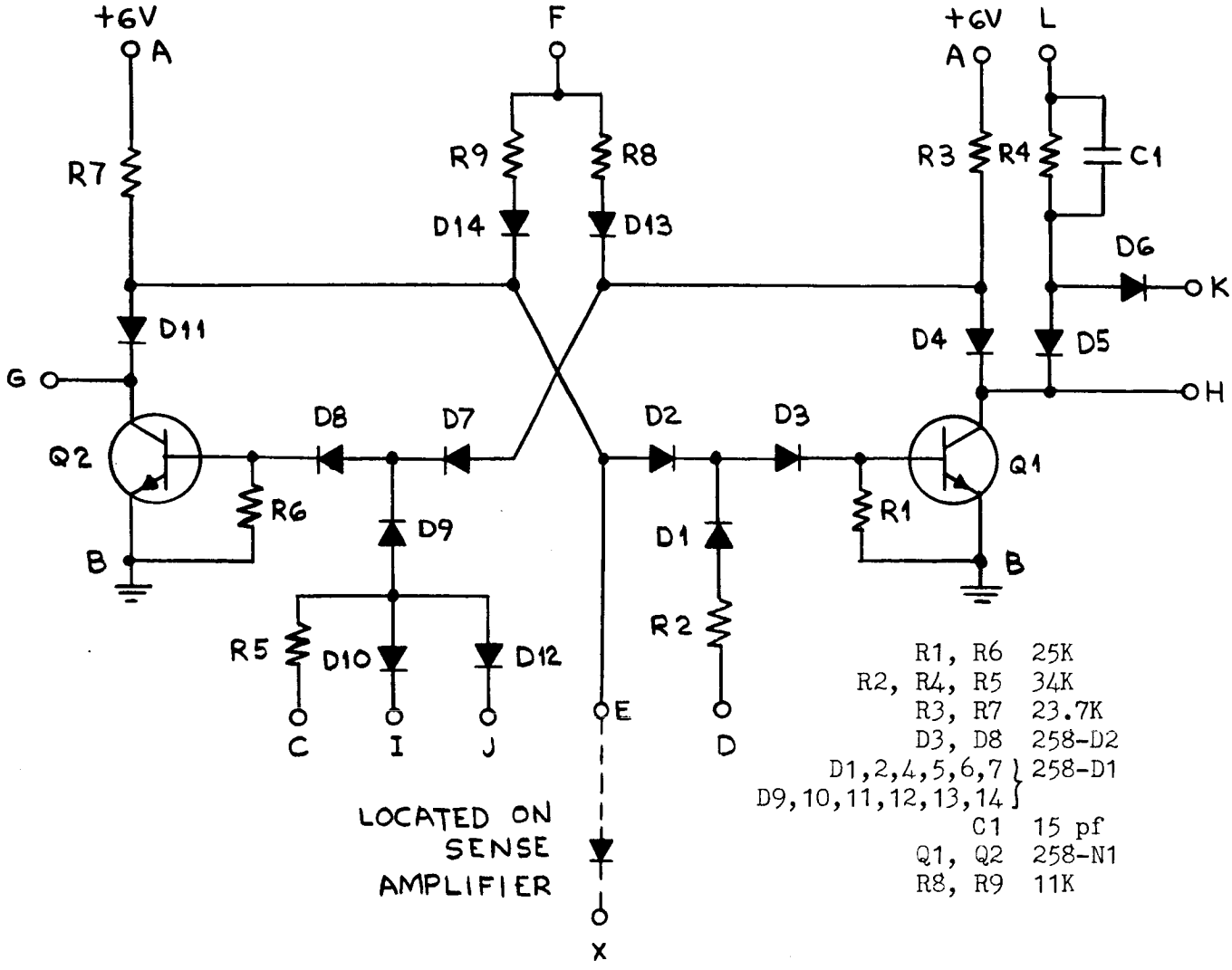

Figure 14

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The information register has a power dissipation of 2 mw per flip-flop. The flip-flop can be set, (Q_2 on, Q_1 off) by pulsing point C to +12 V for 0.5 usec provided the inputs to I and J are more positive than +4 volts. If either I or J are at ground, the input pulse to C will not affect the state of the flip-flop. The flip-flop can also be set by pulsing point E to ground for 0.5 usecond. The flip-flop can be reset by pulsing point D to +12 V for 0.5 usecond. When point L is pulsed, current will flow out thru D6 if the flip-flop is set and will flow thru D_5 instead of out to the load if the flip-flop is reset. Input F is pulsed from ground to +11.2 volts minimum during the time the bit driver is activiated such that the logic output is capable of taking 6.2 ma in the ground state.

10. Output Flip-Flop

This circuit provides an NRZ output at the collector of Q5. When GOC is pulsed, Q3 will conduct if the input to D1 supplies not current. Since Q1 is off Q2 is on and GOC will supply current thru D7 and D5. If the input to D1 supplies current to Q1, Q1 will be on and Q2 off. Therefore, GOC will supply current to D12 and D4 which turns on Q4 and turns off Q3. The collector of Q5 will change only if the input to D1 is different during the interval of the GOC pulse from that during the last GOC pulse.

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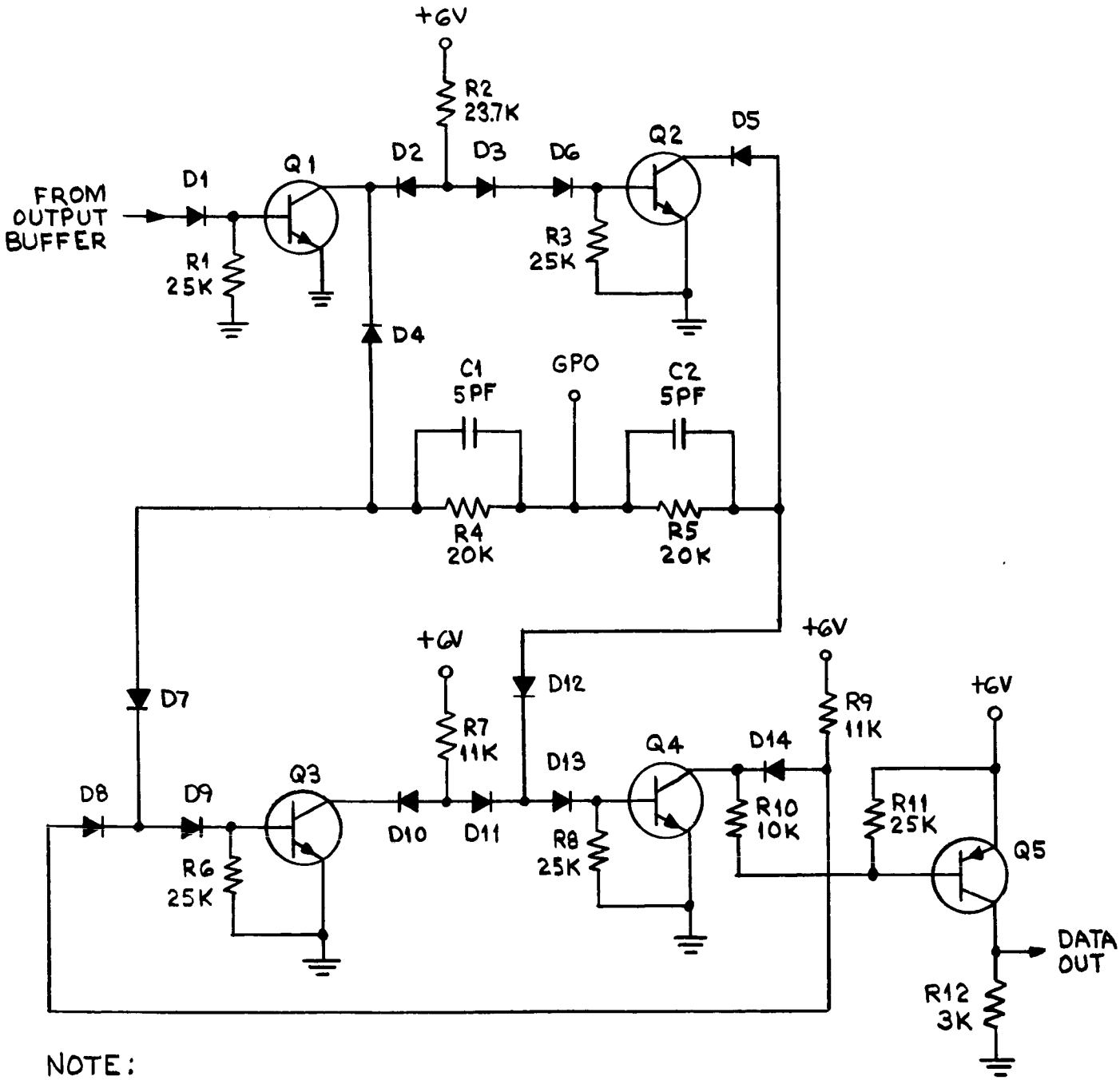

NOTE:
DIODES D1,6,9,13 ARE TYPE 258-D3, ALL OTHERS TYPE 258-D1
TRANSISTOR Q5 TYPE 258-P3, ALL OTHERS TYPE 258-N1

Figure 15

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TECHNICAL REPORT NO. 63

TITLE: READ AMPLIFIER

ENGINEER: C. A. Nelson

UNIT: Advanced Memories

PROJECT NO: 258

DATE: July 30, 1965

ABSTRACT:

This report describes the design of the low power read amplifier designed for the 2.8 million bit memory under contract NAS 5-9518, circuit number 258-015.

Written by: C A Nelson
C. A. Nelson

Approved by: G. A. Fedde
G. A. Fedde

jam

TECHNICAL REPORT NO. 63

I. CIRCUIT SPECIFICATION

The function of the read amplifier is to amplify and detect the plated wire signal and to provide an output signal that indicates whether a "1" or "0" has been detected. The input of the amplifier must reject common-mode signals. The output of the amplifier provides a pulse to the information register if a "1" is detected and no pulse if a "0" is detected. The amplifier is gated during the period of time that the plated wire signal is present at the input, and during all other times no output pulse can occur. The amount of "1" signal required at the input is expressed in terms of volt-seconds because of the integrating function of the amplification stages. The only "0" signal required is that necessary to overcome the noise. The "1" signal requirement is therefore the one which must be met. The following specifications present the functional performance of the read amplifier:

Minimum 1 Signal:	93 mv-ns
Minimum Common Mode Rejection:	28
Maximum Steady-State Power:	3.33 mw
Maximum Input Offset Voltage:	1.56 mv
Maximum Recovery Time from 8 mv offset	3 us
Gate Input Requirements	
"Off" state:	Ground
"On" state:	5.4 volts
Output Requirements	
"0" detected:	+6 volts
"1" detected:	Below 0.42 volts for at least 5us

The remainder of the design requirements will be discussed in the rest of this report.

The circuit is built using thin film resistors. Reference Specification P-HC-06.

II. CIRCUIT DESCRIPTION

The read amplifier is shown in Figure 1. Transistors Q1 and Q2 form a differential amplifier so that common mode signals are rejected and differential signals are amplified. Capacitors have been eliminated in the design of the amplifier wherever possible to make the thin film circuitry as simple as possible. For this reason there is no capacitive coupling between the read amplifier and the bit-sense matrix. When the bit-sense matrix is off, the base currents of transistors Q1 and Q2 flow

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through resistors R1 and R2 respectively. The difference between the steady-state voltages on R1 and R2 is defined as the input offset voltage. When the matrix is switched on this input offset voltage adds to the matrix offset noise to determine the total offset from which the amplifier must recover. Resistors R1 are made fairly low to keep the input offset voltage low, but are high enough so that the signal loss across the bit sense matrix is kept low. Resistors R3 and R4 bias transistors Q1 and Q2 in the linear region. Capacitor C1 provides a signal path between the emitters of Q1 and Q2 and is made high enough to provide a relatively low impedance to the signals being amplified, but is low enough to allow the amplifier to recover from the offset voltage that occurs at the beginning of a memory cycle.

The collector voltages of transistors Q1 and Q2 are made high enough so that the base-collector junctions do not conduct when the bit current is switched during a write cycle. Fairly large transients occur since the output of the bit driver is connected directly to the inputs of the read amplifier. The collector of Q2 is connected directly to the positive 3 volt supply to eliminate high frequency response limitations caused by the Miller effect. When a large transient at the input occurs, either transistor Q1 or transistor Q2 will cut off at a current very low as compared to the bit current, such that there is no significant loading by the amplifier on the bit current other than by resistors R1 and R2.

Transistor Q3 is biased in the linear region to provide signal amplification. The emitter bypass capacitor C2 provides a low impedance path for the signals. The bias currents of transistors Q1, Q2, and Q3 are low to keep the standby power low. The amount of bias current required by these transistors is determined by the amount of low level gain required. This will be discussed after the operation of the rest of the amplifier is explained.

The output of the read amplifier is connected to the information flip-flop. The diode d1 is the logic diode. If a memory "1" is read, transistor Q6, which is normally nonconducting, is turned on to saturation such that its collector swings from +6 volts to nearly -3 volts. When the gate period terminates, Q6 again becomes nonconducting and the collector starts rising towards +6 volts. Capacitor C7 provides a time constant on this voltage rise such that the collector stays below 0.42 volts for 0.5 us to ensure that the information flip-flop will set under worst case conditions. Resistor R13 provides a path for the steady-state collector current of Q5, which is biased in the linear region. The steady-state voltage across R14 is low enough to ensure that the collector of Q5 must swing several tenths of a volt before Q6 begins to conduct. Under severe transient conditions, the collector of Q5 does not move more than 0.2 volts when the gate is off.

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The base-emitter drop of Q6 therefore provides the necessary noise community to ensure that no output will occur in the absence of the gate signal. When a memory "0" is read the input signal is of the opposite polarity and Q6 remains nonconducting such that the information flip-flop remains in the reset state.

When the gate is off, the gate input is at ground potential and transistor Q7 is nonconducting. Transistor Q7 therefore presents a high impedance and for all practical purposes does not affect the performance of the circuit in this state. Two stage negative feedback from the emitter of Q5 to the base of Q4 provides relatively fast transient recovery. Resistor R13 is an order of magnitude higher than R10, so that the two stage current gain of Q4 and Q5 is only slightly greater than unity when the gate transistor Q7 is nonconducting. There are two recovery problems associated with the design of the read amplifier. When the read signal occurs, it is required that the emitter of the gate transistor Q7 be recovered to ground potential in the absence of the read signal. The first recovery problem is caused by the address selection transients that occur near the beginning of a memory cycle. The large "B" selection noise is kept out of the amplifier by leaving the bit-sense matrix off until the word lines selected by the "B" dimension have reached ground potential. This leaves the offset voltage of the bit-sense matrix as the only significant address selection transient. Figures 2a and 2b show the recovery at the emitter of the gate transistor Q7 from an 8 mv offset voltage beginning at the first division, with the read signal occurring at the seventh division. Based on the results of these worst case tests, 3 us should be allowed between the matrix selection and the read out in order that the matrix transient not interfere with the detection of the read signal. This recovery time is controlled by the large negative feedback from Q5 to Q4 and by capacitors C1, C2, C4, and C5.

The second recovery problem is caused by capacitor C5 becoming charged when a "1" signal is read. This results when the gate transistor Q7 is turned on to a low impedance enabling several milliamperes of current to flow through C5 if a "1" signal is being read. When the gate transistor is turned off it is required that the emitter of Q7 return to ground potential before the next read operation. This recovery is controlled by making the C6-R12 and C5 (R8 + R10) time constants short. The recovery is primarily determined by the C5 (R8 + R10) time constant which is less than 20 us, thereby enabling 4 time constants to recover. The C6-R12 time constant is made short (less than 2.5 us) to isolate the collector of Q4 from the base of Q5 during the recovery. Figures 2d and 2e show the voltage at the emitter of Q7 after a "1" and a "0" have been read respectively. As can be seen from Figure 2d, the recovery is nearly complete after 40 us which is well within the 80 us cycle time.

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When Q7 is turned on to a low impedance, the gain through the amplification stages becomes comparatively high. The amount of negative feedback from the emitter of Q5 to the base of Q4 becomes very low since the series impedance of R17 and Q7 is small as compared to the feedback resistor R10 and since a low impedance path is provided at the emitter of Q5. Although the signal levels are higher in the last two stages of amplification than in the first two, the bias currents in the last two stages are lower (approximately 50 ua). Since only the "1" signal must be amplified after the differential stage, the transistors can be arranged such that the "1" signal itself turns the transistors on to a higher level. This allows adequate gain at low bias levels. Since the signal itself turns on the transistor to a lower impedance level, the frequency response of the stage is not limited to its small signal frequency response. The signal levels in Q4 and Q5 (around 300 us and 3 ma respectively) are large as compared to the bias levels of Q1, Q2, and Q3, and this fact enables Q4 and Q5 to be biased at lower levels and still have respectable gain, and at these signal levels the gain of Q4 and Q5 is relatively stable with variations of bias current.

The low impedance of Q7 to the signal is guaranteed by specifying the saturation resistance of Q7 to be 50 ohms maximum at I_B = 1 ma, I_E = 0. The "1" signal also turns Q7 on in the forward direction such that the effective resistance to the "1" signal is approximately 15 ohms. Capacitor C8 provides the charge to clean up the charge stored in Q7 during the first 3.5 volts of the fall of the gate input. Resistor R7 provides a means of adjusting the gain of the amplifier. The amplifier is designed to allow detection of the minimum plated wire signal at a signal to noise ratio of 2:1 under worst case conditions with a value of R17 equal to zero.

As indicated previously, the gain of Q1, Q2, and Q3 is strongly a function of their bias currents. The small signal gain is limited by the frequency response of the stages at the low bias currents, even though the lowest capacitance transistors available are being used. This gain variation could be partially stabilized by lower resistances shunting the signal path. Additional power would be required to make up for the resulting gain loss. All of the shunt resistors (R5, R7, R8, R11, and R12) have been made as large as the design limitations allow so that the gain is maximized for a given power level. The bias levels of Q1, Q2, and Q3 were determined experimentally to give the desired gain. In one sense the high frequency response limitations of these stages is helpful in that the amplifier integrates the plated wire signals. This means that except for the loss due to the resistance of the plated wires, the detection of the read signals is independent of the length of the sense line, assuming the noise is invariant. This also means that for a given length of sense line, the detection is practically independent of the position of the bit along the sense line, except that the amplifier outputs can occur earlier for the bits at the ground end.

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Typical amplifier response to the read out signals is shown in Figure 2a. The rise time of the word current is about 150 ns and the fall time about 40 ns. The signal which occurs during the fall of the word current is being detected in this memory. The negative signal at the fall of the word current is the "1" signal. The reason the "1" signal does not return to the base line is primarily due to the charging of capacitor C5 by the "1" signal. When reading on the fall time of the word current, the amplifier must be allowed to recover from the turn on signal. As seen in Figure 2a this recovery time is approximately 250 ns. It can also be seen that the amplifier undershoots from the turn on signal so that some benefit is obtained from the turn on signal. A word current width of 400 ns appears to be ideal. Figure 2a was obtained by reading a bit near the amplifier on a 10 foot sense line. Because of the reflected component of the plated wire signal, the signal at the input of the amplifier peaks at two different times. These peaks do not appear in Figure 2a because of the integration function the amplifier performs. It is important to note that when viewing the read signals in the amplifier, the waveshape is not the same as that on the input.

The gate timing should be wide enough to envelop the read signals. The gate input should be up to 90% of its high state within 30 ns after the start of the word current fall, since there is 20 ns delay through the amplifier and since the amount of signal developed during the first 10 ns of the word current fall is insignificant. Leaving the gate on until 170 ns after the start of the word current fall will enable the read signals to be completely enveloped for a 10 foot sense line and a 40 ns word current fall time. The gate should not be left on any longer than necessary to provide maximum noise immunity.

III. COMPONENTS AND DERATING

The following is the list of the components used in the circuit shown in Figure 1.

R1, R2	400 ohms
R3, R4, R7	24 K ohms
R5	15.8 K ohms
R6, R11	32 K ohms
R8, R12	10 K ohms
R9, R13, R15	48 K ohms
R10, R16	4K ohms
R14	1 K ohm
C1	560 pf
C2, C4, C5	1000 pf
C3, C6	200 pf
C7	81 pf
C8	27 pf
Q1 thru Q4, Q7	2N3493
Q5	2N3251
Q6	2N2501
d1	1N3207

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A total resistor tolerance of ±5% is used in the design. The tolerance includes initial tolerance of ±1%, temperature variation of ±1.5% (±300 ppm over a ±50°C range), and ±2.5% variation for life. A total matching tolerance of 3% has been assumed.

A tolerance of ±20% has been used for the capacitors whose values are 200 pf or greater. This includes ±10% initial tolerance, ±5% for temperature variation over the range of -20°C to +80°C, and ±5% variation for life. No matching was assumed.

The transistor parameters used in the design are obtained from the Motorola data sheets. The class A current gain of the transistors has been derated 20% for life variation. The class A base-emitter drops have only been derated for temperature variation at 2.5 mv/°C.

The 3 volt supplies have been assumed not to vary more than ±0.1 volt, and the 6 volt supply has been assumed not to vary more than ±0.2 volt.

IV. POWER REQUIREMENTS

The standby power required by the read amplifier has been calculated assuming infinite transistor betas for ease of calculation. The calculated power is not more than 1% too high. The standby power is calculated by first determining the emitter currents of all the class A transistors, and then multiplying the currents by the supply voltage from which they come.

Equation 1 $$\overline{I_{E2}} = \overline{I_{E1}} = \frac{\overline{E_{-3}} - V_{BE1}}{R_3}$$

$$= \frac{3.1 - 0.5}{(.95)(24 \times 10^3)}$$

$$= 114\ \mu a$$

Equation 2 $$\overline{I_{E3}} = \frac{\overline{E_{-3}} + \overline{E_{+3}} - \overline{I_{E1}} R5 - V_{BE3}}{R_6}$$

$$= \frac{3.1 + 3.1 - (114 \times 10^{-6})(15.8 \times 10^3)(.97) - 0.5}{(.95)(32 \times 10^3)}$$

$$= 130\ \mu a$$

Equation 3 $$\overline{I_{E5}} = \overline{I_{E4}} = \frac{\overline{E_{-3}} - V_{BE4}}{R9} = \frac{3.1 - 0.5}{(48 \times 10^3)(.95)}$$

$$= 57\ \mu a$$

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The standby power is given by

Equation 4 $$P_{SS} = E_{-3}(I_{E1} + I_{E2} + I_{E3} + I_{E4} + I_{C5}) + E_{+3}(I_{C1} + I_{C2} + I_{C4} + I_{E5}) + E_{+6}I_{C3}$$

With the assumed infinite transistor betas, the collector currents are equal to their respective emitter currents.

Equation 5
$$\begin{aligned} P_{SS} &= 3.1\,(114 + 114 + 130 + 57 + 57) \times 10^{-6} \\ &\quad + 3.1\,(114 + 114 + 57 + 57) \times 10^{-6} + 6.2\,(130) \times 10^{-6} \\ &= 3.1\,(472 \times 10^{-6}) + 3.1\,(342 \times 10^{-6}) + 6.2\,(130 \times 10^{-6}) \\ &= 1.46 \times 10^{-3} + 1.06 \times 10^{-3} + 0.81 \times 10^{-3} \\ &= 3.33 \text{ mw} \end{aligned}$$

Equation 5 also shows that the currents required from the -3, +3, and +6 volt supplies are 472, 342, and 130 ua respectively.

The transient power at a 80 us cycle time is less than 0.07 mw. This power is used to drive the gate transistor and to charge capacitor C7 if a "1" is being read. The total power required can, therefore, be stated as 3.40 mw.

V. DESIGN EQUATIONS

A. Bias Conditions

The base-collector junctions of Q1 and Q2 are reverse biased to prevent them from conducting when a fast 1.5 volt transient occurs on the input. This transient exists when the bit current is being switched during the write cycle. The class A response of the transistors is slow enough that the design requirement is met by steady state biasing, and this requirement determines the maximum value of resistor R5. The steady state collector voltage of Q1 plus the amount the base-collector junction can be forward biased before it conducts significant current must be less than 1.5 volts. The steady state collector voltage of Q1 is:

Equation 6
$$\begin{aligned} V_{C1} &= E_{+3} - \overline{I_{C1}}\ \overline{R5} \\ &= 2.9 - (114 \times 10^{-6})(0.98 \times 15.8 \times 10^{3}) \\ &= 1.14 \text{ volts} \end{aligned}$$

where $\overline{I_{C1}}$ is obtained from Equation 1. The base-collector junction will not conduct a significant current, as compared to the bit current, when forward biased by 0.36 volts so that the required design condition has been met.

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The lower limit of resistor R7 is determined from the design condition that the class A base-collector junctions be reverse biased by one volt to be well within the linear region of the transistor characteristics for amplification purposes. The maximum base voltage at Q3 is:

Equation 7 $$\overline{V_{b3}} = \overline{E_{+3}} - \underline{I_{C1}R5}$$

$$= \overline{E_{+3}} - \frac{\overline{E_{-3}} - \overline{V_{BE1}}}{\overline{R3}} \quad \underline{R5}$$

$$= 3.1 - \frac{3.1 - 0.6}{(.98)\ (24 \times 10^3)} \quad (.95 \times 15.8 \times 10^3)$$

$$= 1.50 \text{ v}$$

The maximum collector current of Q3 is:

Equation 8 $$\overline{I_{C3}} = \frac{\overline{E_{-3}} + \overline{V_{b3}} - \underline{V_{bE3}}}{\underline{R6}}$$

$$= \frac{3.1 + 1.50 - 0.5}{.95 \times 32 \times 10^3}$$

$$= 138\ \mu a$$

The minimum collector voltage of Q2 is:

Equation 9 $$\underline{V_{C3}} = \underline{E_6} - \overline{I_{C3}}\ \overline{R7}$$

$$= 5.8 - (138 \times 10^{-6})(.98 \times 24 \times 10^3)$$

$$= 2.55 \text{ v}$$

The minimum reverse bias of the base-collector junction of Q3 is therefore:

Equation 10 $$\underline{V_{Cb3}} = \underline{V_{C3}} - \overline{V_{b3}}$$

$$= 2.55 - 1.60$$

$$= 0.95 \text{ volts}$$

such that the desired design condition has been met.

The collector-base junction of Q4 is also to be reverse biased by one volt. Since the base is at ground potential

Equation 11 $$\underline{V_{Cb4}} = \underline{E_{+3}} - \overline{I_{C4}}\overline{R11}$$

$$= 2.9 - (57 \times 10^{-6})(.98 \times 32 \times 10^3)$$

$$= 1.1 \text{ volt}$$

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such that the design condition has been met.

Since, as discussed previously, the steady state drop across R14 is small (0.06 v), the collector-base junction of Q5 is sufficiently reverse biased.

B. Input Offset Voltage

The input offset voltage is the difference between the steady state voltages across resistors R1 and R2. These voltages are caused by the base currents of Q1 and Q2 flowing through R1 and R2 respectively. Under balance conditions the input offset voltage is zero. The input offset voltage is expressed as

Equation 12 $$V_{io} = \pm \left[\frac{(\overline{E_{-3}} - \overline{V_{BE1}})\ \overline{R1}}{\overline{R3}\ (\overline{H_{FE1}} + 1)} - \frac{(\overline{E_{-3}} - \overline{V_{BE2}})\ \overline{R2}}{\overline{R_4}\ (\overline{HFE2} + 1)} \right]$$

$$= \pm \left[\frac{(3.1 - 0.5)\ (1.05)\ (400)}{(1.02 \times 24 \times 10^{\#})\ (23)} - \frac{(3.1 - 0.6)\ (1.02)\ (400)}{(1.05 \times 24 \times 10^{3})\ (110)} \right]$$

$$= \pm 1.56 \text{ mv}$$

This offset voltage is included in determining the total offset voltage that occurs when the bit-sense matrix is selected.

C. Common Mode Rejection

The common mode rejection is performed by the differential transistor stages Q1 and Q2 and is defined as the ratio of the output signal of Q1 when a differential signal is applied to the output signal of Q1 when a common mode signal of the same amplitude is applied. The common mode rejection is primarily important during the time the read signal is present so that the common mode word noise is rejected. The word noise is of high enough frequency that the emitter coupling capacitor C1 may be considered a short circuit. The common mode rejection then becomes only a function of R3, R4 and the input impedances of Q1 and Q2. The common base input impedance of a transistor is given by

Equation 13 $$h_{ib} = \frac{k}{I_E} \quad \frac{T}{T_M}$$

where k is a constant measured at a given absolute temperature, T_M, and where T is the absolute temperature. The transistors have a maximum k of 30×10^{-3} at 25°C. Let

Equation 14 $$C = \frac{kT}{T_M}$$

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Then at 80°C the maximum Cis 36.3×10^{-3}. The common mode rejection can now be quite accurately expressed as

Equation 15 $$CMR = \frac{E_{-3} - \overline{V_{BE2}}}{2C_2}$$

$$= \frac{2.9 - 0.84}{2 \times 36.3 \times 10^{-3}}$$

$$= 28$$

Equation 15 is valid only where R3 and R4 are equal and where Equation 13 is valid. Equation 13 will hold true for bias currents up to one to three milliamps. Equation 15 is interesting in that is shows that the only way to increase the common mode rejection is to increase the emitter supply voltage. The common mode rejection obtained is sufficient, however, since the common mode noise that occurs during the detection of the plated wire signal has the same order of magnitude as the signal.

D. Gate Drive Requirements

The gate circuit, which is comprised of Q7, C8, and R16 is designed to be driven from a circuit whose steady state levels are ground and +5.4 volts minimum in the "on" and "off" states respectively. The minimum base current supplied by the gate drive to Q7 should be greater than 1 ma to assure that Q7 is in the low impedance state desired. The minimum base current is

Equation 16 $$\underline{I_{b7}} = \frac{5.4 - \overline{V_{bC7}}}{R16}$$

$$= \frac{5.4 - 1.14}{(1.05)\ (4 \times 10^3)}$$

$$= 1.01 \text{ ma}$$

as desired. The gate drive circuit is assumed to have a maximum voltage in the "on" state of 6.1 volts. The maximum base current which the gate drive circuit must supply to each read amplifier is

Equation 17 $$\overline{I_{b7}} = \frac{6.1 - V_{bC7}}{\underline{R16}}$$

$$= \frac{6.1 - 0.6}{.95 \times 4 \times 10^3} = 1.45 \text{ ma}$$

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The value of C8 is determined by the amount of charge that must be supplied to neutralize the charge stored in the gate transistor Q7. The amount of this charge is

Equation 18 $$\overline{Q_8} = \overline{I_{b7}} \left(\overline{Ts} + \frac{\overline{T_F}}{2}\right)$$

where Ts is the charge storage time constant of Q7 and T_F is the desired fall time. Substituting and solving

$$\overline{Q_8} = 1.45 \times 10^{-3} \left(50 \times 10^{-9} + \frac{10 \times 10^{-9}}{2}\right)$$

$$= 80 \times 10^{-12}$$

It is desired that this charge be supplied within the first 3.5 volts of the fall of the gate voltage so that there is sufficient charge remaining to snap the gate transistor off. The amount of voltage change required to supply the charge is

Equation 19 $$\overline{\Delta V} = \frac{\overline{Q_8}}{C_8}$$

$$= \frac{80 \times 10^{-12}}{0.85 \times 27 \times 10^{-12}} = 3.48 \text{ volts}$$

so that the design condition has been met.

E. Duration of Output to Information Flip Flop

The collector of Q6 is required to be below 0.42 volts for 0.5 us to ensure that the information flip-flop will set under worst case conditions when a "1" has been read. When a "1" is read, transistor Q6 saturates and discharges capacitor C7 to nearly -3 v. C7 is flowing from the 6 v supply through resistor R15 and the load resistor, R_L, which is in the information flip-flop. The charging of C7 is made slow enough to ensure that the collector of Q6 is below 0.42 volts for at least 0.5 us. When transistor Q7 turns off after C7 has been discharged the charge of the collector voltage with respect to time is determined from Equation 20.

Equation 20 $$C \frac{d v_{c7}}{dt} + v_{c7} \left(\frac{1}{R15} + \frac{1}{R_L}\right) - \left(\overline{E_6} + E_{-3} - \overline{V_{cE7}}\right)\left(\frac{1}{R15} + \frac{1}{R_L}\right) + \frac{V_{d1}}{R_L} = 0$$

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where V_{cE7} is the voltage at which Q7 saturages and V_{d1} is the forward drop of diode d1. Solving this equation and inserting the initial conditions gives the collector voltage of Q7 after it turns off as

Equation 21 $v_{c7} = -2.6 + 8.5\ (1 - e^{-t/1.04 \times 10^{6}})$

The time between the time at which the collector voltage of Q7 falls below 0.46 volts during the discharge of C7 and the time at which Q7 turns off is at least 50 nanoseconds. Therefore, the collector voltage of Q7 must be below 0.46 volts for 450 nanoseconds after Q7 turns off to meet the required design condition. Substitution into Equation 21 gives

$$v_{c7} = 0.37 \text{ volts} \quad @ \quad t = 450 \text{ ns}$$

so that the required design condition has been met.

VI. SIGNAL DETECTION

The transistor amplification stages have extremely limited frequency response and nonlinear characteristics because of the low current levels at which they are biased. Because of these facts, calculated response to the read signals would be extremely difficult. The detection of the read signals has, therefore, been determined by worst case measurements. These measurements were performed over the required temperature range of -20°C to +80°C with ±10% supply variations used to simulate end of life resistor tolerance plus the supply voltage tolerance. The maximum signal required for detection was 93 mv-ns at 80°C. This is approximately the amount of volt-seconds that will be received by the read amplifier from a 4 mv plated wire signal on a ten foot sense line.

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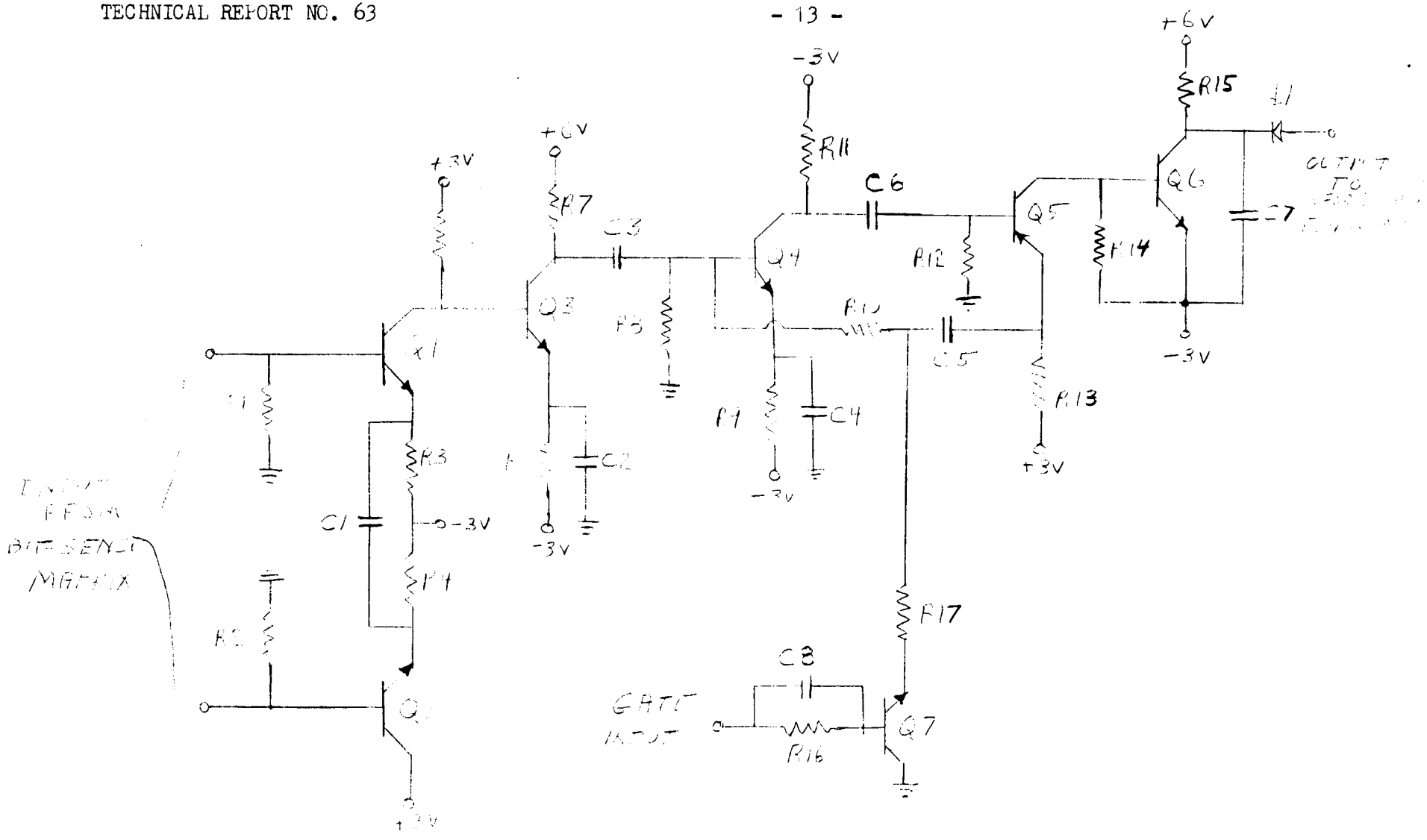
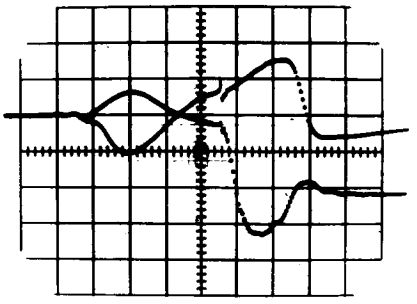
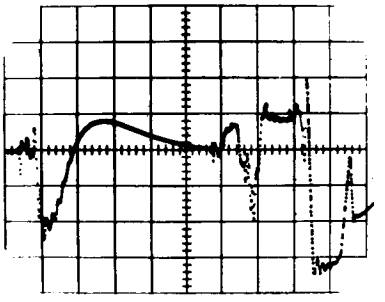


FIGURE 1

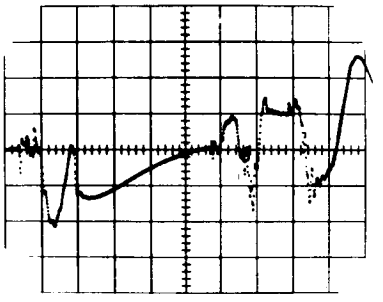
READ AMPLIFIER SCHEMATIC



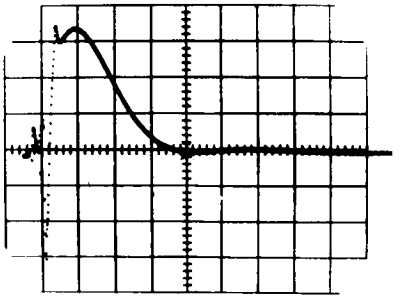
a. Taken at base of Q5.
Shows the "1" and "0" readout signals.
Horizontal scale: 100 NS/Div.
Vertical scale: 200 MV/Div.



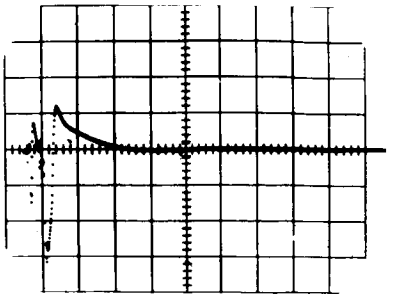
b. Taken at emitter of Q7.
Shows the recovery from a -8MV matrix offset applied to Q2.
Horizontal scale: 0.5 μSEC/Div.
Vertical scale: 200 MV/Div.



c. Taken at emitter of Q7.
Shows the recovery from a +8MV matrix offset applied to Q2.
Horizontal scale: 0.5 μSEC/Div.
Vertical scale: 200 MV/Div.



d. Taken at emitter of Q7.
Shows recovery from a "1" read signal between cycles.
Horizontal scale: 10 μSEC/Div.
Vertical scale: 200 MV/Div.



e. Taken at emitter of Q7.
Shows recovery from a "0" read signal between cycles.
Horizontal scale: 10 μSEC/Div.
Vertical scale: 200 MV/Div.

Figure 2. Waveforms in the Read Amplifier

TECHNICAL REPORT NO. 66

TITLE: BIT-SENSE MATRIX

ENGINEER: C. A. Nelson

PROJECT: 258

CONTRACT: NAS 5-9518

UNIT: Advanced Memories

DATE: August 4, 1965

ABSTRACT:

The design of the bit-sense matrix switch is described in this report. The bit-sense matrix is comprised of these low level switches which provide a low impedance between the selected plated wire in a bit group and the read amplifier and bit driver.

Submitted by: C A Nelson
C. A. Nelson

Approved by: G. A. Fedde
G. A. Fedde

jam

TECHNICAL REPORT NO. 66

Circuit Design Report: BIT-SENSE MATRIX

Circuit No: 258-017

Written by: C. A. Nelson

Approved by: G. A. Fedde

I. CIRCUIT FUNCTION

The bit-sense matrix selects the plated wire from which information is to be read during a read cycle or into which the information is to be written during a write cycle. The bit-sense matrix is comprised of a group of transistor switches (see Figure 1). There is one such switch for every plated wire and dummy wire. Normally these switches present a high impedance. During a read cycle one of the switches in series with a plated wire is turned on to a low impedance so that the read signal from the plated wire is connected to one side of the differential amplifier which is the first section of the read amplifier. A dummy wire is connected to the other side of the differential amplifier such that rejection of common mode noise is obtained. There is, however, some noise which can couple through the capacitance of the matrix switches which are off. The balanced bit-sense matrix is used to provide cancellation of this noise, the number of switches connected to each side of the differential amplifier, which is the first stage of the read amplifier, being made equal. When a plated wire on one side of the matrix is selected, the dummy wire on the other side is used by turning on its matrix switch.

The problem that arises with the balanced bit-sense matrix is that if the same information is represented by the same polarity of signal on both sides of the balanced matrix, the read amplifier will detect the information differently for the different sides of the matrix. One solution to this problem would be to reverse the information coming from one side of the matrix after it has been detected. The use of the transformer at the output of the bit driver, however, writes the information in such a manner that it will be detected properly such that no additional circuitry is necessary to reverse the information.

The polarity of the signal stored in a plated wire is dependent upon the polarity of the bit current. Thus a positive bit current will write one polarity and a negative bit current will write the opposite polarity. The information to be written is determined by which bit driver transistor switch (S1 or S2) is closed. Closing one of the switches will cause a positive current to flow to one side of the matrix

and a negative current to the other because of the transformer action. Therefore, closing one of the switches will write the same information with opposite polarities through the different halves of the matrix and the information will be detected correctly by the read amplifier.

II. CIRCUIT SPECIFICATION

In the unselected state the matrix circuit must present a high impedance to the bit current transients and to the plated-wire signals. The following list sets forth the basic specifications of the matrix circuit when selected:

Maximum small-signal impedance:	10 ohms
Maximum differential offset voltage:	6.5 mv
Maximum drop to bit current:	0.3 volts
Maximum average power at 2 us serial bit rate:	37 mw/us

The power is expressed in terms of the amount of time the matrix circuits are on during the memory cycles, since different timing is used for the read and write cycles.

III. COMPONENTS AND DERATING

The components used in the matrix circuit shown in Figure 2 are as follows:

R1, R2	2.36 K $\pm$1%
R3	135 ohms $\pm$1%
Q1	258-C1
Q2	258-C2

The circuit is being built using thin film resistors and chip transistors. The transistors are being purchased to the base-emitter breakdown and beta specifications. The rest of the parameters shown on the transistor specifications are arrived at by an evaluation of the transistor characteristics.

In the design of the circuit the resistors are derated 4%. The transistor betas are derated 70% and the transistor base-emitter saturation voltage is derated 50 mv. The 0.1 volt to 0.3 volt drop across the matrix transistors to the 35 ma bit current is determined by an evaluation of the transistors.

IV. CIRCUIT DESIGN

The two basic functions that a matrix circuit must perform when it has been selected are that it must pass the bit current with a low voltage drop during a write operation and it must present a low impedance to the plated wire signal during a read operation. A matrix circuit is selected by applying simultaneous positive and negative balanced pulses to the base resistors of Q1 and Q2 respectively. The amount of base current needed for the operation of the circuit is determined by the transistor betas such that the drops across the circuit when the bit current is less than the specified maximum drop. The value of the base resistors is determined under worst case conditions to give a minimum base current of 2 ma such that the transistors are operated at 50% of their room temperature beta at 35 ma of bit current. Transistor Q2 passes the positive bit current and Q1 passes the negative bit current.

When the selection pulses are applied, practically all the base current flows through the collectors of the transistors. The transistors, therefore, with nothing applied to the emitters are operated in the saturation region at zero emitter current. In this state, the collector-emitter small signal characteristic is essentially a pure resistance, termed the saturation resistance. The impedance presented to the plated wire signal by the matrix circuit is the parallel combination of the saturation resistances of Q1 and Q2. This impedance is made low by having a maximum 10 ohm saturation resistance of Q2 at the minimum base current.

The maximum base current to the transistors is calculated to be 2.81 ma under worst case conditions. This current is used in determining the drive requirements of the matrix driver (Circuit 258-029), and the power requirements as presented in that circuit report.

When the bit current is switched, a maximum transient of 2.1 volts will occur at the output of the bit driver. In order to prevent sneak currents flowing in the unselected wires the base-emitter junctions of the unselected wires are reverse biased by 3 volts. The unselected switches therefore present a high impedance to signals as large as can occur during operation of the memory.

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BIT-SENSE MATRIX
258-017
C. A. Nelson

Resistor R3 is used to terminate the plated wires. This resistor (135 ohms) in parallel with the 400 ohm input impedance of the differential amplifier terminates the selected wire in its characteristic impedance of 100 ohms to prevent reflections of the read signals. The unselected wires are terminated in R3 to provide a low noise level during the read operation.

The shunt capacitance presented by the unselected matrix transistors at their common connections must be low so as not to give reactive reflections of the read signal. For an average base-emitter junction capacitance of 4.5 pf, there is a total of 72 pf shunting the input to the amplifier. The time constant seen by the read signals at the input to the amplifier is the shunt capacitance times half the characteristic impedance (since the lines are terminated in the characteristic impedance) and is therefore 3.6 nanoseconds. Since this time is short as compared to the switching time of the read signal, the effect of the shunt capacitance is one of delaying the signals by the time constant and does not result in a significant loss of signal amplitude.

The final consideration in the design of the matrix circuit is that it must have low noise when switches on so as not to interfere with the detection of the read signal. The read signal occurs 3 us after the selection of the matrix switch to allow the amplifier to recover from the selection noise. The noise generated when the matrix circuit is selected can be considered as the sum of two components. The first component is the switching transient, which is caused by unbalances between the matrix transistor capacitances and between the rise times of the positive and negative selection pulses. This transient lasts for less than 100 ns and causes no significant recovery problems in the amplifier. The second component of selection noise is the differential offset voltage which appears as a step of voltage at the input of the amplifier and is caused by steady state unbalances. There are three sources of the differential offset voltage which can be added to give a close approximation of the differential offset voltage.

The first source of differential offset voltage is the difference in voltage which exists at the common emitter connection of the matrix transistors due to the base-emitter leakage currents flowing through the 400 ohm shunt resistors at the input of the differential amplifier. For a difference of 10 nanoamperes per switch at 25°C, this gives a 1.2 mv difference in voltage at 80°C. The second component of differential offset voltage is the difference between the emitter offset voltages of the PNP transistors of the selected matrix switches. Since the

saturation resistance of the NPN transistors is an order of magnitude higher than that of the PNP transistors, the emitter offset voltage of the PNP transistor is the offset voltage of the matrix switch. The emitter-offset voltage is defined as the emitter collector voltage at zero emitter current and a specified base current. The difference in emitter-offset voltages between two PNP transistors can be as large as 1.5 mv. The final component of differential offset voltage exists due to an unbalance in the selection current. This unbalance current flows down the plated wire, and the voltage is due to the resistive drop across the plated wire. The unbalance current is caused by unbalances in the base resistors and in the base-emitter drops of the transistors. For each base current being off tolerance 2% with a 16 ohm sense line, the resulting differential voltage unbalance is 3.2 mv. The sum of the three components of the differential offset voltage is therefore 5.9 mv which is less than the specified maximum amount.

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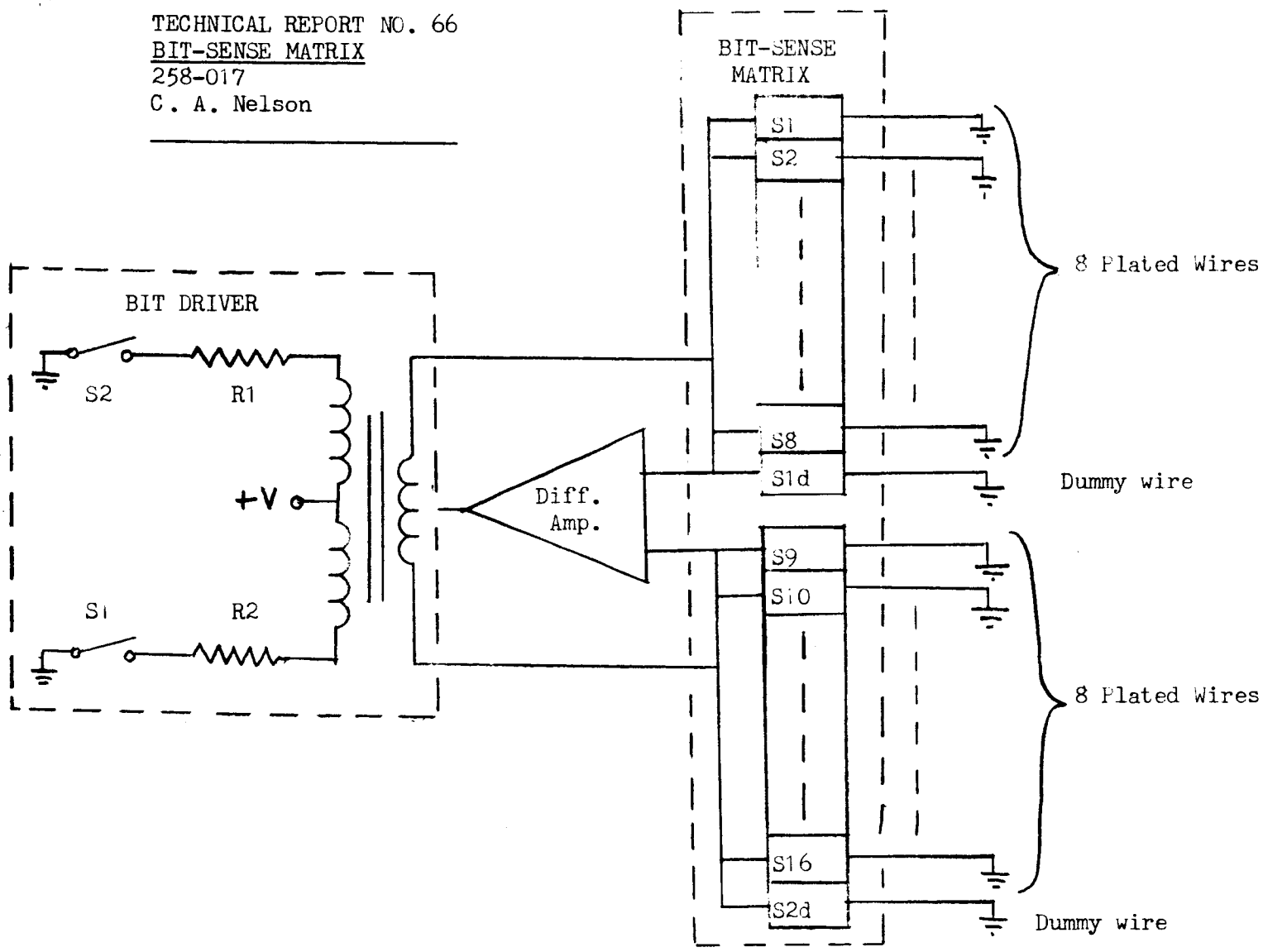

FIGURE 1

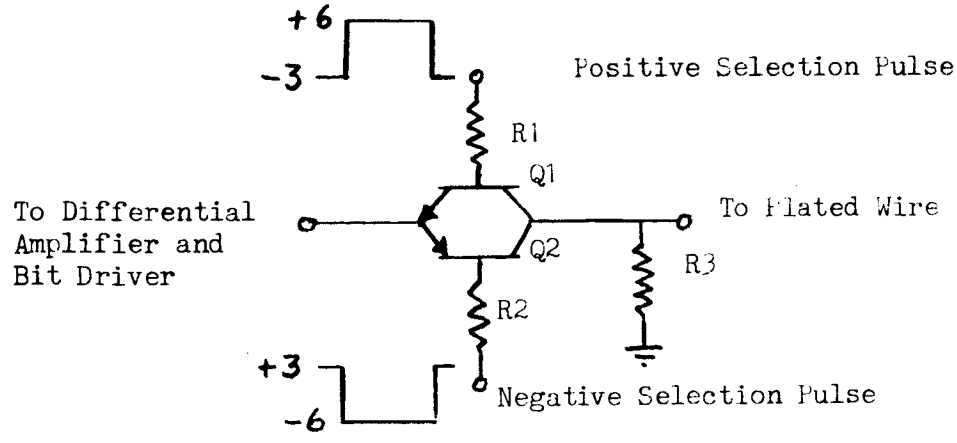

FIGURE 2

Bit-Sense Matrix Circuit

TECHNICAL REPORT NO. 62

TITLE: BIT DRIVER

ENGINEER: C. A. Nelson

UNIT: Advanced Memories

PROJECT NO: 258

DATE: July 29, 1965

ABSTRACT:

The bit driver, circuit number 258-016, designed for the 2.8 million bit memory under Contract NAS5-9518 is discussed in this report.

Written by: C A Nelson
C. A. Nelson

Approved by: G. A. Fedde
G. A. Fedde

jam

TECHNICAL REPORT NO. 62

I. CIRCUIT SPECIFICATION

The function of the bit driver is to drive pulses of current down the plated wire during the memory write cycle. This current in time and spatial coincidence with the word current writes new information in the plated wire. The phase modulated method of writing is used to write information so that the bit driver must supply two pulses of current, one following the other. If a "1" is to be written the first current pulse is of one polarity and the second of the opposite polarity. The polarities of the current pulses is reversed if a "0" is to be written. The time at which the pulses occur in the memory cycle is controlled by two timing pulses. Two logic inputs from the information register determine whether a "1" or a "0" is to be written. These inputs are the collectors of the two transistors in the information register. The performance and requirements of the bit driver are given as follows:

Output Current:	35 ma $\pm$6.2%
Balance Tolerance:	$\pm$4.3%
Output Current Rise Time:	30 ns maximum
Output Current Fall Time:	40 ns maximum
Turn-on Delay:	15 ns maximum
Turn-off Delay:	20 ns maximum

Timing Input Drive Requirements

"Off" state:	-3 volts
"On" state:	11.1 volts min., 13 ma min.

Timing Input Switching Time Requirements

Rise Time:	10 ns maximum
Fall Time:	20 ns maximum

Logic Input Requirements

Low State:	0.35 volts maximum at 6.2 ma
High State:	1 ua maximum at 3 volts
Maximum Power:	215 mw at 2 us serial bit rate

The switching times of the bit current are given for the bit driver driving a short line. Four times the delay of the bit line should be added to obtain the rise time of the bit current. The switching times and delays were determined experimentally under worst case conditions.

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July 30, 1965

II. COMPONENTS AND DERATING

The schematics of the bit driver is shown in Figure 1. All the components except resistors R1, R2 and the transformer are packaged in the thin film circuit P-HC-02. The thin film resistors are derated 4%. Semiconductor diode drops are determined from the semiconductor specifications and derated by 50 mv. The transistor betas are derated 40%. The precision resistors R1 and R2 are derated 1%. The following is a list of the components used in the bit driver.

R1, R2	255 ohms, $\pm$0.1%
R3, R4	2.7 K, $\pm$1%
R5 thru R8	1.73K, $\pm$1%
d1 thru d10	258-D1
Q1, Q2	258-N1

Figure 2 shows the steady-state load on the output of the bit driver, components Q1, Q2, R1, R2 and 258-T1 being the same as shown in Figure 1. Resistors R_{S1} and R_{S2} are the shunt resistors at the input of the read amplifier. V_m represents the saturation voltage drop across the bit-sense matrix transistors, and R_{S3} and R_{S4} are the shunt resistors in the bit sense matrix which terminate the plated and dummy wires. Resistors R_{S1} through R_{S4} are thin film resistors and are derated 4%. R_L represents the resistance of the sense line. The following are the values used in determining the bit current.

R_{S1}, R_{S2}	400 ohms, $\pm$1%
R_{S3}, R_{S4}	135 ohms, $\pm$1%
R_L	16 ohms
V_m	0.1 volts min; 0.3 volts max

III. CIRCUIT DESCRIPTION AND DESIGN EQUATIONS

When the bit timing pulses are in their low state at -3 volts, diodes d7 thru d10 are all reverse biased so that bit driver, except for the diode capacitance, does not affect the operation of the information register. The base-emitter junctions of Q1 and Q2 are reverse biased by 3 volts and are therefore not conducting, except for a small amount of leakage current. With the bases of the transistors on minus 3 volts and the bit timing pulses at minus 3 volts there is no current flowing through diodes d1 through d6. Except for a small amount of leakage current, therefore, there is no current flowing in the circuit and the standby power is essentially zero.

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The outputs of the information are arbitrarily labeled "0" and "1" for purposes of this report. If a "0" is to be written into the memory the "0" output will be low and the "1" output will be high, and if a "1" is to be written into the memory the "1" output will be low and the "0" output will be high. The state of the information register is set prior to the application of the bit timing pulses.

The bipolar bit current is obtained by turning on one transistor to a saturated state when the first timing pulse is applied and then turning on the other transistor when the second timing pulse is applied. Opposite polarities of current are obtained by having the polarities of the primary windings opposite to each other with respect to the output winding. When Q1 is turned on current flows from the 12 volt supply, through the primary winding to R1, through R1 and to the collector of Q1. The transformer windings all have a 1:1 ratio with respect to each other such that the output current is equal to the collector current of the conducting transistor. The load voltage is relatively low as compared to the 12 volt supply, such that the output current magnitude is primarily determined by precision resistors R1 and R2.

The logical operation of the circuit will be described assuming a "1" is to be written into the memory, so that the "1" output of the information register is low and the "0" output is high. When Bit Timing Pulse 1 is applied Q1 is turned on and Q2 is kept off. To keep Q2 off the voltage at the base of Q2 must be less than 0.3 volts so that there is practically no base current to Q2. At this voltage resistor R4 can conduct up to 1.13 ma so that the maximum allowable current through d2 and d5 from the Bit Timing Pulse is 1.13 ma. After finding the minimum junction drops of d2 and d5 at this current, the maximum allowable voltage at the anodes of d5 and d9 is 1.12 volts. At this voltage maximum current through R6 from the Bit Timing Pulse is 7.3 ma. The information register must therefore be capable of taking 6.2 ma in the low state. The maximum junction drop of d9 plus the .35 volt maximum information register gives a maximum voltage at the anodes of d5 and d9 of 1.04 volts. Since this is less than the maximum allowable voltage to assure that Q2 remains nonconducting the required design condition has been met. The function of diode d2 (and d1) is to act as a level shifter to assure that Q2 remains nonconducting.

Transistor Q1 is turned on when the information register is in the "1" state since the "0" output is in the high state so that all the current flowing from the bit timing pulse through R5 flows through d4 and d1 to the base of Q1. The minimum base current under worst case conditions is calculated to be 2.66 ma. For 40 ma of collector current, the transistor is therefore operated at a beta of 15 which is less than the minimum derated transistor beta of 20.

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When the bit timing pulse goes low, clean up current is supplied to the base of Q1 from the -3 volt supply through resistor R3. The amount of current necessary to turn off Q1 within the specified time was determined experimentally to be 1.2 ma. The value of R3 was calculated to give this amount of clean up current under worst case conditions.

When Bit Timing Pulse 2 is applied, (still assuming the information register to be in the "1" state), Q2 is turned on and Q1 remains off since the connection of diodes d7 and d10 to the information register is reversed with respect to d8 and d9. If the information register is in the "0" state, the sequence in which transistors Q1 and Q2 turn on is reversed.

The maximum current that the Bit Timing Pulse must supply has been calculated to be 13.0 ma under worst case conditions.

IV. BIT CURRENT TOLERANCE

The equation for determining the bit current, I_b, is determined from the circuitry shown in Figure 2. Assuming Q1 to be the conducting transistor the bit current is given by

$$I_b = \frac{\frac{E_{12} - V_{CE1} - V_m}{R1} - \frac{V_m}{R_{S1}}}{1 + R_L \left(\frac{1}{R_{S1}} + \frac{1}{R_{S3}} + \frac{2}{R1} \right)}$$

where E_{12} is the value of the 12 volt supply voltage and V_{CE1} is the saturation drop across Q1. In calculating the bit current tolerance E_{12} was allowed to vary $\pm 1\%$ and V_{CE1} between 0.1 volt and 0.3 volt. The rest of the parameters were allowed to vary as described in Section II of this report. Substituting the parameters gives a total tolerance on the bit current of $\pm 6.2\%$ and a balance tolerance of 4.3%, the balance tolerance referring to the difference between the two polarities of current.

V. TRANSFORMER DESIGN

The 258-T1 transformer is built by winding two windings of equal turns using bifilar wire. One of the bifilar wires in each winding is connected to form primary windings. The remaining wires of each winding are connected in parallel to form the output winding. The transformer therefore has very low leakage inductance from each priming winding to

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the output winding, and the capacitance between the bifilar wires does not limit the switching time since the change of voltage across the output winding is the same as the change of voltage across the secondary winding. The resulting transformer as a switching time of a few nanoseconds and presents no significant limitation on the switching time of the bit current.

The number of turns is determined by the condition that the transformer droop be less than 2% under worst case conditions. The maximum steady-state voltage that appears across the primary winding is

$$\bar{E}_p = 2(I_b R_L + \bar{V}_m) = 1.72 \text{ volts}$$

The minimum allowable magnetizing conductance of the transformer for a 2% droop is

$$\underline{L_m} = \frac{\bar{E}_p \, \bar{t}}{(.02)\underline{I_p}} = 650 \text{ uh}$$

for t = 300 ns. The transformer is built using a CF-102 size torroid (Indiana General) made of T-1 material. With this torroid 36 turns are required under worst case conditions to give the minimum allowable magnetizing inductance.

VI. POWER REQUIREMENTS

As previously discussed there is no standby power required by the bit driver. The pulse power required while writing at a 2 us serial bit rate is:

$$P = 2 \, \frac{E_{12}(\bar{I}_{TC} + \bar{I}_p)}{2 \times 10^{-6}} \, t$$

where I_{TC} is the current supplied by the timing clock, I_p is the current flowing in the primary winding and t is the duration of the timing pulse. Substituting into the equation gives

$$P = 715 \, t \text{ mw}$$

where t is in us. For a 300 ns current pulse the required power is 215 mw. It should be noted that this is the power required by all the bit drivers for information being written at a 2 us serial rate.

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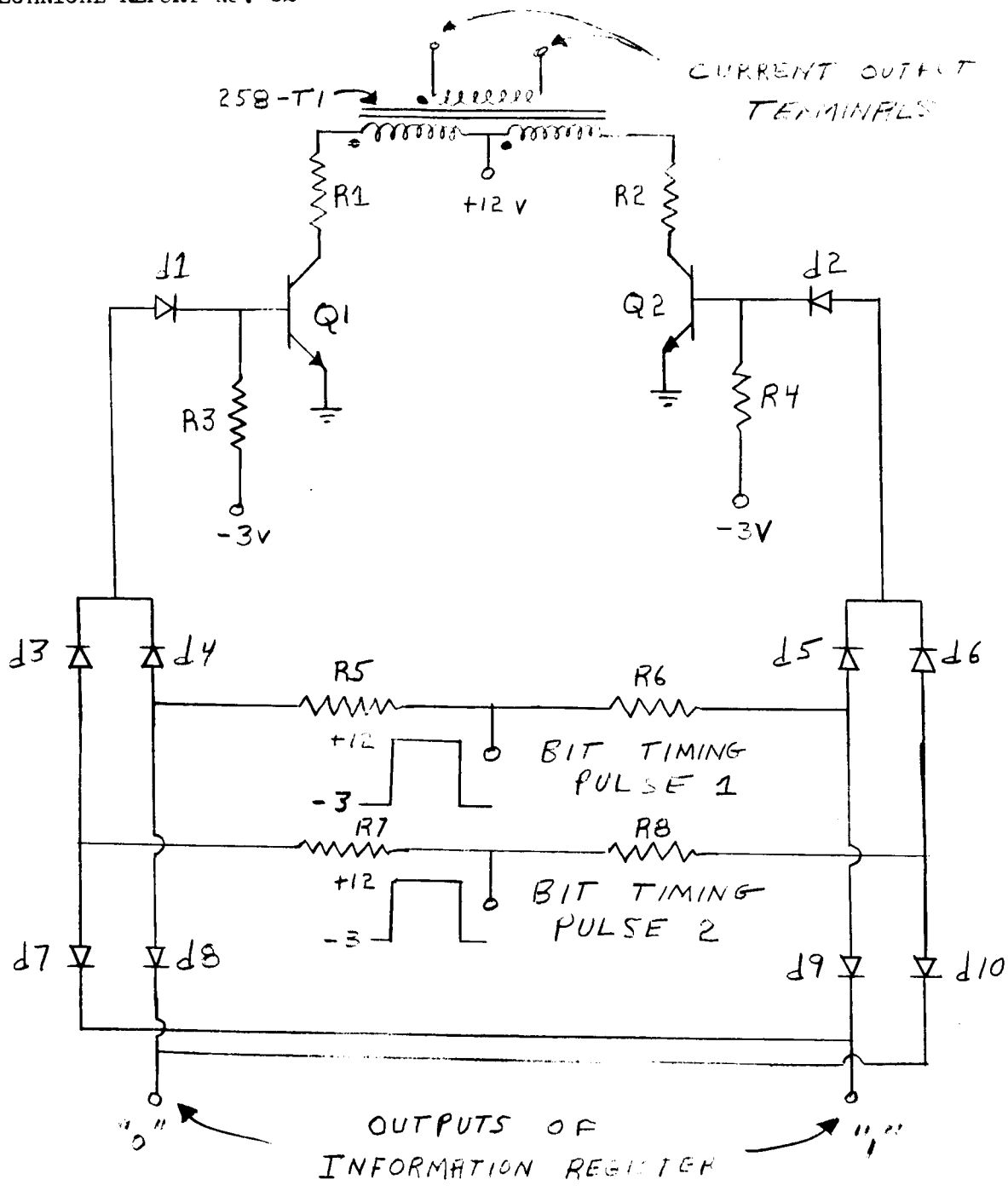

FIGURE 1

BIT DRIVER SCHEMATIC

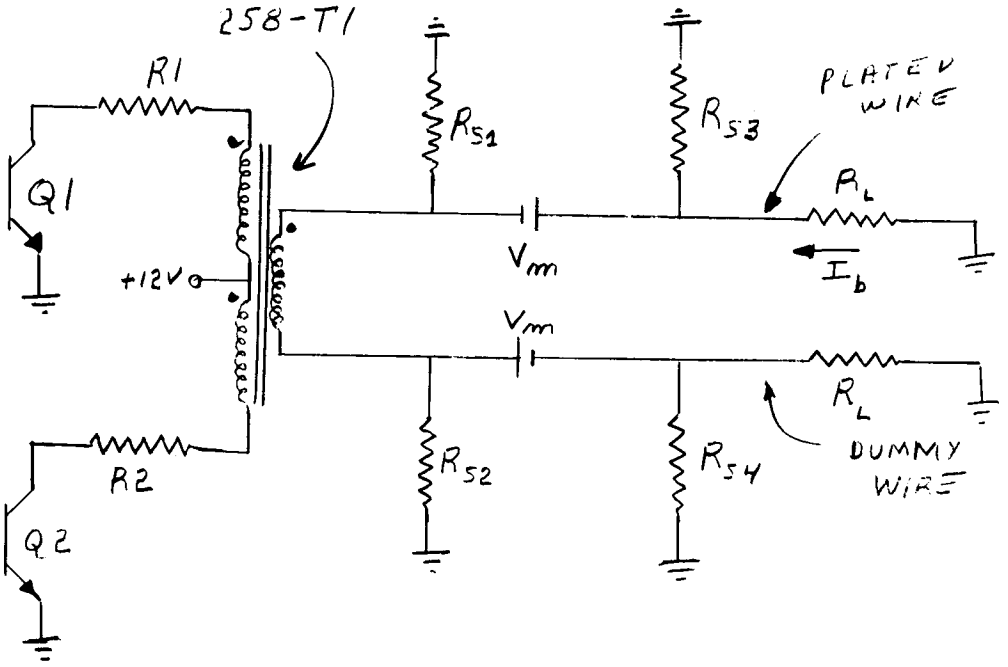

FIGURE 2

CIRCUITRY INVOLVED IN DETERMINING THE BIT CURRENT

TECHNICAL REPORT NO. 68

TITLE: MATRIX DRIVERS

ENGINEER C. A. Nelson

PROJECT: 258

CONTRACT: NAS 5-9518

UNIT: Advanced Memories

DATE: August 3, 1965

ABSTRACT:

This report describes the circuits which are used to drive the selected bit-sense matrix switches. The circuit is designed to drive 40 matrix switches in parallel.

Submitted by: C A Nelson
C. A. Nelson

Approved by: G A Fedde
G. A. Fedde

jam

TECHNICAL REPORT NO. 68

I. CIRCUIT SPECIFICATION

The purpose of the matrix driver is to supply the pulses which select the matrix switches that are turned on in the memory cycle. (Reference Bit-Sense Matrix Report, Circuit number 158-017). The matrix drivers are capable of driving 40 matrix switches in parallel, since 40 bit parallel operation is used when reading from or writing into the memory stack. The matrix driver supplies positive and negative going balanced pulses as shown in the schematic. The output pulses must swing to six volts minimum with respect to ground and be able to supply 2.81 ma per load, or a total of 112 ma. The input current required from the counter which selects the matrix position is 22.7 ma.

II. COMPONENTS AND DERATING

Semiconductor junction drops have been derated 100 mv and the transistor betas have been derated 70%. The resistors have been derated 4% in case the circuit is built using thin film resistors. All components are operated at less than 50% their rated voltage levels. The following is a list of the components used in the schematic:

R1, R2	50 ohms $\pm$1%
R3	422 ohms $\pm$1%
R4	10 K $\pm$ 1%
C1, C2	1 uF, 20 v
Q1	258-N1
Q2	258-P2
d1 thru d12	258-D1

III. CIRCUIT DESCRIPTION AND DESIGN

The plated wire matrix drivers are driven from a 16 stage counter, each stage driving one matrix driver. Only the matrix driver driven by the conducting stage of the counter is activated such that only the desired matrix switches connected to the plated wires are turned on. When base current is supplied to Q1 from the counter, Q1 saturates and its collector swings from 12 volts to the saturation drop across Q1. There is therefore nearly a 12 volt swing across the 70 turn primary

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August 3, 1965

winding of the transformer. The number of turns of the secondary winding (57) is determined to give a minimum pulse output of 6 volts with respect to ground under worst case conditions. The number of turns of the primary was calculated to assure that the torroid (Indiana General T1 material, CF102 size) does not saturate for a 5 us pulse.

At the termination of the input pulse transistor Q1 becomes nonconducting and the output pulses terminate. Diodes d9 and d10 provide a recovery path for the magnetizing current of the transformer.

The R1-C1 network is placed in series with the supply voltage to provide protection against an accidental turn on of Q1 for a long period of time. Should this happen the transformer would saturate and without R1 nothing would limit the collector current of Q1 and it would burn out. C1 is used to provide a low impedance to the supply voltage under normal operation. For a flight model R1 and C1 should be eliminated since it would be more desirable to have Q1 burn out than have R1 dissipate 3 watts of power.

The dummy matrix driver selects the matrix switches in series with the dummy wires that are to be turned on. If one of the 8 plated wire matrix switches on one side of the balanced bit-sense matrix is turned on, the dummy matrix switch on the other side is to be turned on. (See the Bit-Sense Matrix circuit report.) This is accomplished by an eight input diode "or" gate (diodes d1 through d8), the inputs being driven by the collectors of the transistors of the appropriate plated wire matrix drivers.

Resistor R3 is chosen to supply enough base current (20 ma minimum) such that Q2 is operated at a beta of 10. The operation of the dummy matrix driver is identical to that of the plated wire matrix driver except that the collector of Q2 swings from ground to nearly 12 volts when Q2 is turned on.

The maximum load current of each secondary is 112 ma. Reflected to the primary this becomes 182 ma. The maximum magnetizing current of the transformer is 16.8 ma for a 4 us pulse width. The maximum collector current of Q2 is therefore slightly less than 200 ma so that the transistor is operated at a beta of 10.

The maximum current which will flow through d1 is calculated to be 2.7 ma under worst case conditions. The maximum collector current of Q1 is therefore 227 ma, so that 22.7 ma of input current is required to operate the transistor at a beta of 10.

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The power supplied to and dissipated by the bit-sense matrix is the load current reflected to the primary (182 ma) times the 12 volt supply minus the load current times the 3 volt supply, since the return path for the load current is through the 3 volt supplies. This gives 37 mw/us for a 2 us serial bit rate.

The total power required by the matrix drivers at an 80 us repetition rate is

$$P = \frac{E_{12} (\overline{I_m} + \overline{I_{d1}})}{80 \times 10^{-6}} t$$

where I_m is the transformer magnetizing current. On the read cycle the matrix will be on for approximately 4 us, and on the write cycle the matrix will be on for approximately 1 us. At these pulse widths the magnetizing current is 16.8 ma and 4.2 ma, and the power required is calculated to be 26 mw and 5 mw respectively. The input current has not been included in the power calculations.

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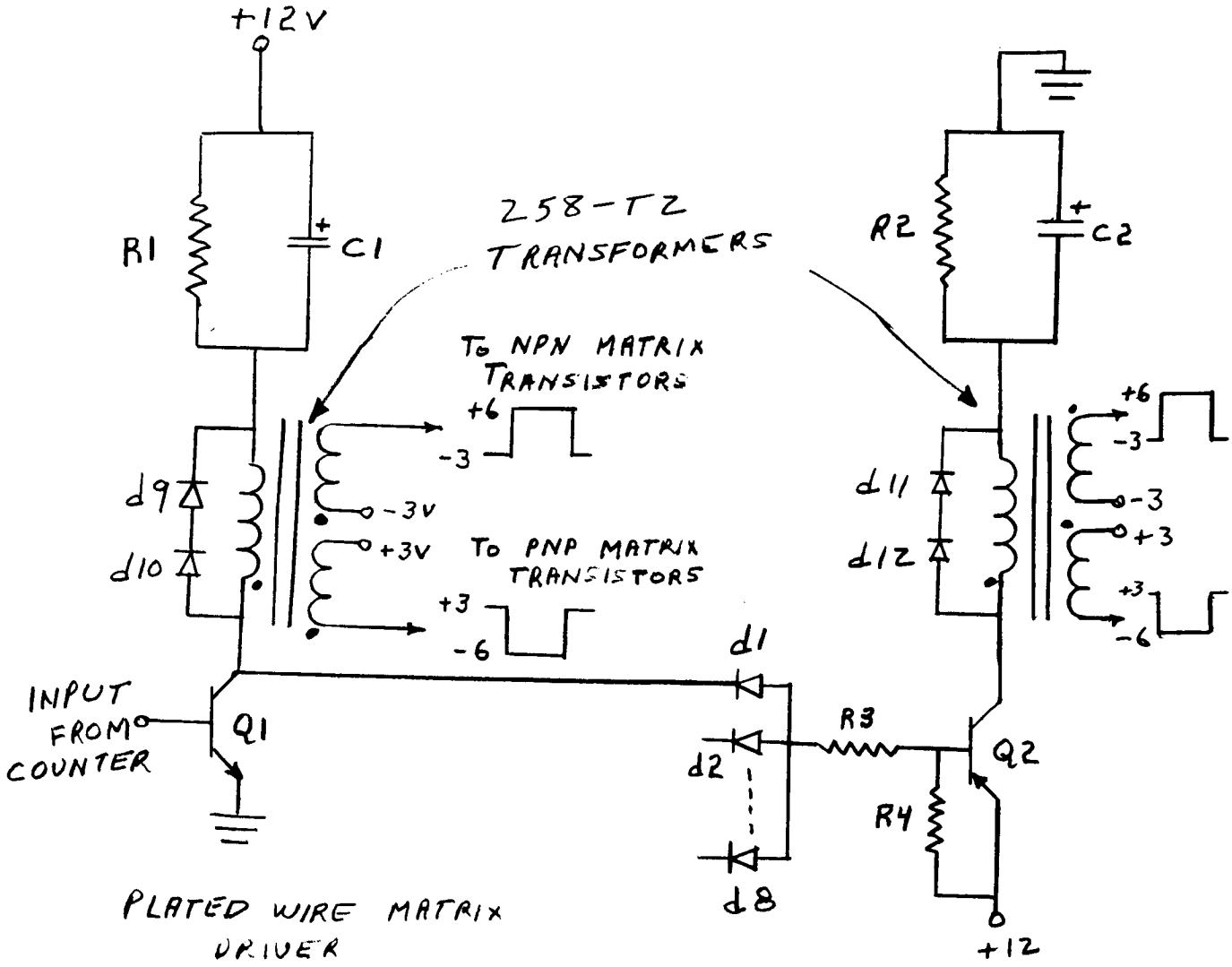

SCHEMATIC OF MATRIX DRIVERS

TECHNICAL REPORT NO. 70

TITLE: Bit Path Interface Circuits

ENGINEER: C. A. Nelson

PROJECT: 258

CONTRACT: NAS 5-9518

UNIT: Advanced Memories

DATE: August 6, 1965

ABSTRACT:

This report describes the design of the Bit Power Pulser, Bit Timing Pulser, and the Read Gate Pulser. The three circuits are driven by delay flops which provide the pulse timing. The Bit Power Pulser provides the pulse which steps up the current level of the information register. The Bit Timing Pulser provides the pulse which activates the Bit Driver. The Read Gate Pulser provides the pulse which drives the read amplifier gates.

Submitted by: C. A. Nelson

Approved by: G. A. Fedde

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I. BIT POWER PULSER

The function of the bit power pulser is to provide the voltage pulse which steps up the current level of the information registers. The output must swing from ground to 11.1 volts minimum and be capable of supplying 2.1 ma to each information register, or a total of 84 ma since the circuit drives the power pulse input of 40 information registers. The bit power pulser is driven from a delay flop.

In the circuit shown in Figure 1, the input is normally at ground potential. Q1 is, therefore, normally nonconducting and the base of Q2 is at 12 volts. Q2 is, therefore, also off and the circuit requires no standby power. With Q2 off the output is at ground potential by means of resistor R4.

When the timing pulse from the delay flop is applied to the input transistors Q1 and Q2 saturate and the output voltage swings to the 12 volt supply voltage minus the saturation drop across Q2. The minimum output voltage is greater than the minimum required output voltage of 11.1 volts. Resistor R2 is chosen such that Q2 is operated at a beta of 12 under worst case conditions. Resistor R1 is chosen such that Q1 is operated at a beta of 15 under worst case conditions.

The output voltage will switch to the high state within 100 nanoseconds after the application of the input pulse. The output voltage can stay high for approximately 1 us after the input returns to ground due to the charge stored in Q2. Since there is approximately 6 us before the information register will be reset, no discharge circuitry is necessary.

The resistors have been derated 4% should the circuit be built using thin film resistors. The following is a list of the components used in the circuit shown in Figure 1.

R1	4.22 K ohms $\pm$1%
R2	866 ohms $\pm$1%
R3	500 ohms $\pm$1%
R4	1.00 K ohms $\pm$1%
Q1	258-N1
Q2	258-P2

II. BIT TIMING PULSER

The function of the bit timing pulser is to provide the voltage pulse which activates the bit drivers. The output must swing from minus 3 volts to 11.1 volts minimum and be capable of supplying 13 ma to each bit driver, or a total of 520 ma to the 40 bit drivers. The timing of the pulse is provided by a delay flop which drives the input of the bit timing pulser.

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The worst case switching times were determined experimentally. The output voltage has maximum rise and fall times of 10 and 20 nanoseconds respectively and maximum turn-on and turn-off delays of 10 and 40 nanoseconds respectively.

The circuit is shown in Figure 2. The input signal is normally at ground and all the transistors are nonconducting. The circuit, therefore, requires no steady state power. With Q3 nonconducting the output is at minus 3 volts as desired by means of resistor R4.

When the timing pulse from the delay flop swings positive transistors Q1 and Q3 switch to the saturated state. The output voltage, therefore, swings to the 12 volt supply voltage minus the saturation drop across Q3. The minimum output voltage is greater than the minimum required output voltage of 11.1 volts. Resistor R2 is chosen such that Q3 is operated at a maximum beta of 10 under worst case conditions. Capacitor C2 is used to obtain fast turn-on of Q3. Resistor R1 is chosen such that Q1 is operated at a maximum beta of 20 under worst case conditions. Capacitor C1 is used to obtain fast turn-on and turn-off of Q1.

The purpose of Q2 is to provide current to neutralize the charge stored in Q3 when the input from the delay flops goes to ground. The R3-C3 time constant is made small enough (68 nanoseconds maximum) such that C3 is charged to the input voltage by the time the input swings back to ground (greater than 200 nanoseconds). When the input swings to ground, the charge stored in C3 provides turn-on base current to Q2 and the resulting collector current of Q2 flows to the base of Q3. The value of C2 is chosen such that the minimum charge stored in C2 times a Q2 beta of 20 is equal to the maximum amount of charge stored in Q2.

The resistors have been derated 4% should the circuit be built using thin film resistors and the capacitors have been derated 5%. The following is a list of the components used in the circuit shown in Figure 2:

R1	2.26 K ohms $\pm$1%
R2	365 ohms $\pm$1%
R3, R4	1.00 K ohms $\pm$1%
C1, C2, C3	56 pf $\pm$10%
Q1	258-N1
Q2	258-P2
Q3	2N-3467

III. READ GATE PULSER

The function of the read gate pulser is to provide the voltage pulse which drives the read amplifier gates. The output must swing from ground to 5.4 volts minimum and be capable of supplying 1.45 ma to each gate. In addition, the output must be capable of driving 31 pf per gate. The timing

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of the pulse is provided by a delay flop which drives the input of the read gate pulser. The switching times of the circuit were measured under worst case load conditions. The rise and fall times were measured to be 10 and 15 nanoseconds respectively, and the turn-on and turn-off delays (50% of input to 50% of output) were measured to be 10 and 8 nanoseconds respectively.

A partial schematic of the read gate pulser is shown in Figure 3. The output circuit drives 10 read amplifier gates. There are a total of four output circuits (not shown) which are driven in parallel by Q1, Q2, and Q3 to provide the output pulses to the 40 read amplifier gates.

The input signal from the delay flop is normally at ground and all the transistors are nonconducting. The circuit, therefore requires no steady state power. The output of the circuit is normally at ground by means of resistor R10.

When the input signal swings positive transistors Q1 and Q6 switch to the saturated state. The output voltage, therefore, swings to the 6 volt supply voltage minus the saturation drop across Q3. The minimum output voltage is greater than the minimum required output voltage of 5.4 volts. Resistor R9 is chosen such that Q6 is operated at a maximum beta of 16. Capacitor C5 was chosen to give a fast turn-on of Q6 and to supply enough transient base current to Q6 to charge the load capacitance. Resistor R2 was chosen such that Q1 is operated at a maximum beta of 15 under worst case conditions. Capacitor C2 was chosen to obtain fast turn-on and turn-off of Q1 and to supply enough transient base current to Q1 to supply the transient base current to four Q6 transistors.

The purpose of Q5 is to provide current to neutralize the charge stored in Q6 when the input pulse terminates. The purpose of Q4 is to provide a low impedance path to discharge the load capacitance. When the input pulse switches back to the ground state, transistors Q2, Q3 and Q4 switch to the saturation state, and Q1 turns off. Capacitor C6 was chosen to obtain fast turn-on of Q5 and to provide sufficient transient base current to Q5 to supply enough current to the base of Q6 to neutralize the charge stored in Q6. Capacitor C4 was chosen to obtain fast turn-on of Q4 and to provide sufficient transient current to the base of Q4 to enable Q4 to discharge the load capacitance. Capacitor C3 was chosen to obtain fast turn-on of Q3 and to provide sufficient transient current to the base of Q3 to enable Q3 to supply the transient base current to four Q5 transistors.

When the input pulse is applied, capacitor C1 stores charge which is used to turn on Q2 when the input pulse returns to ground. The R1-C1 time constant (34 nanoseconds maximum) is made short as compared to the

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pulse width (greater than 100 ns) so that C1 has sufficient time to store the charge. The value of C1 was determined to give fast turn on of Q2 and to supply sufficient transient current to the base of Q2 to enable Q2 to provide the required transient current to Q3 and to four Q4 transistors. After C1 ceases to supply base current to Q2, transistors Q2, Q3, Q4, and Q5 and the circuit returns to its steady state condition.

Resistors R3, R4, R5, R6, R7, and R9 are used to provide steady state biasing and leakage current paths. The same component derating was used as in the Bit Timing Pulser. The following is a list of components used in the circuit shown in Figure 3.

R1	500 ohms ±1%
R2	4.42 K ohms ±1%
R3 thru R7, R9	10.0 K ohms ±1%
R8	3.01 K ohms ±1%
R10	1.00 K ohms ±1%
C1, C4, C5	56 pf ±10%
C2	43 pf ±10%
C3, C6	27 pf ±10%
Q1, Q3, Q4	258-N1
Q2, Q6	258-P3
Q5	258-P1

IV. TEST RESULTS

The above circuits were tested using worst case load conditions. The supply voltages were varied ±10% to simulate worst case supply voltage variations and resistor tolerances. Except for varying the voltage level of the output pulse the circuit performance was unaffected.

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August 6, 1965

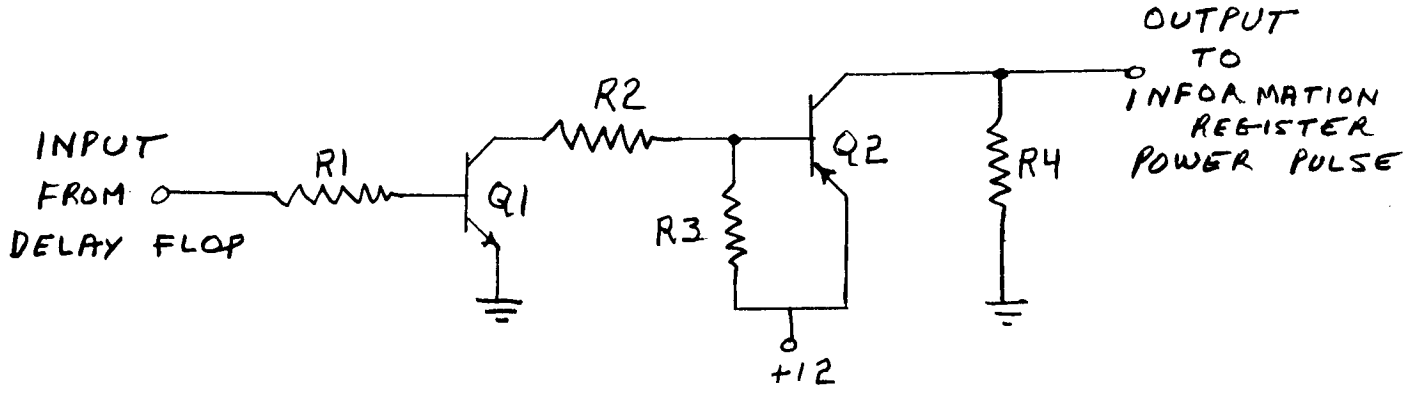

FIGURE 1
BIT POWER PULSER

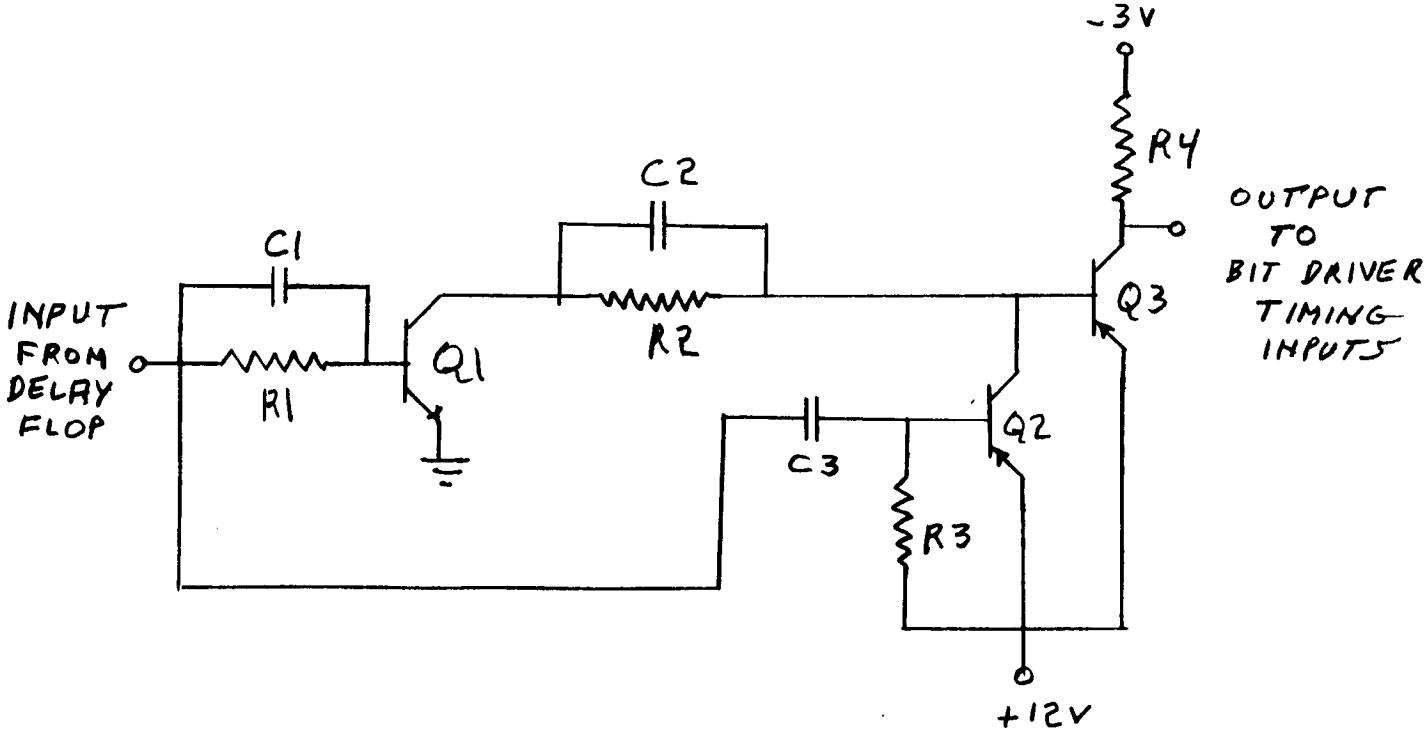

FIGURE 2
BIT TIMING PULSER

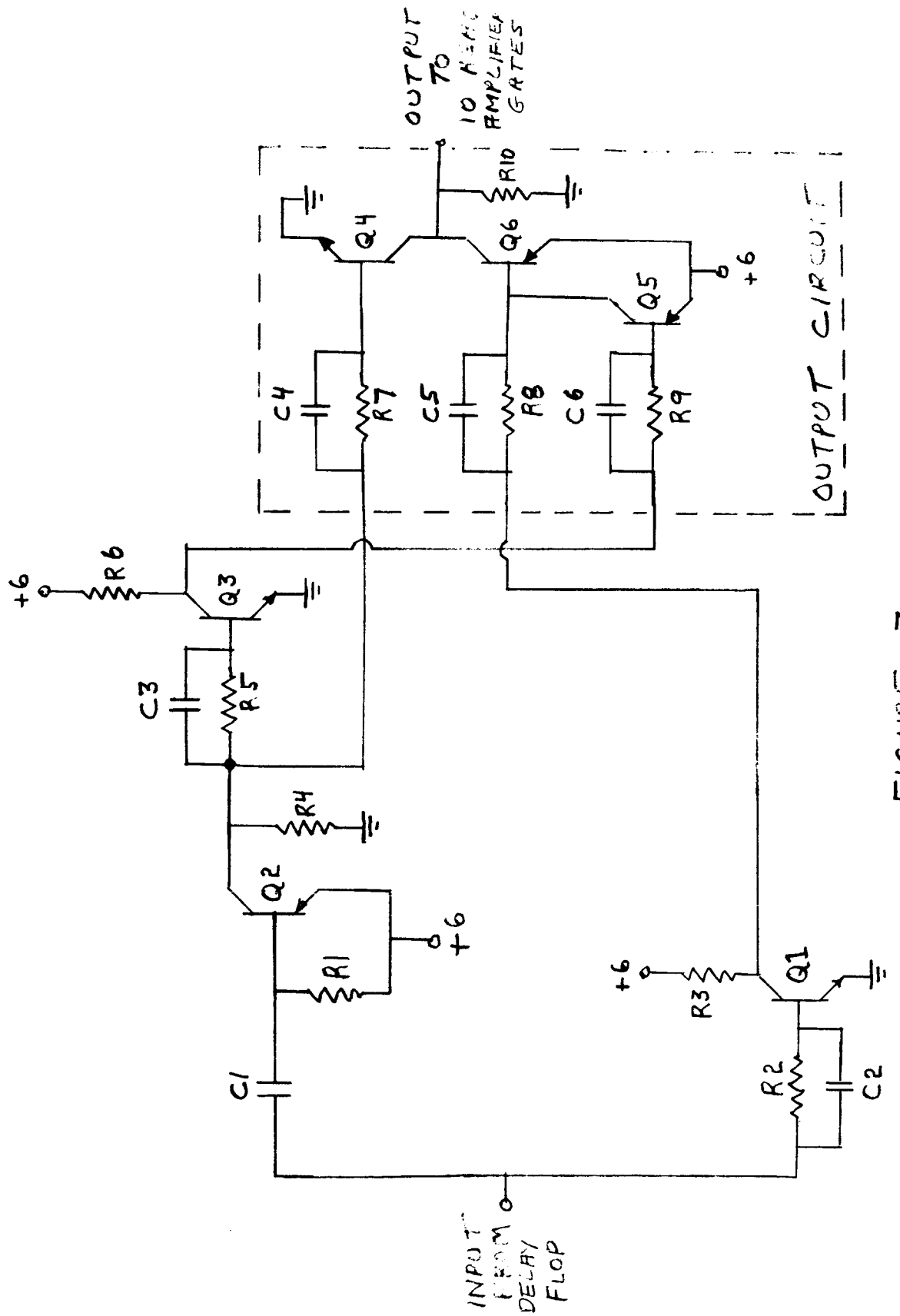

FIGURE 3

PARTIAL SCHEMATIC OF READ GATE PULSER

TECHNICAL REPORT NO. 69 (Interim)

TITLE: WORD CURRENT SOURCE

ENGINEER: R. Mosenkis

PORJECT: 258

CONTRACT: NAS 5-9518

UNIT: Advanced Memories

DATE: August 5, 1965

ABSTRACT:

The Word Current Source is a pulsed current regulator which provides a high-amplitude word current with fast fall time to the memory. This report discusses the design philosophy and operation of this circuit.

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Approved by: G. A. Fedde
G. A. Fedde

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TECHNICAL REPORT NO. 69

1. INTRODUCTION

The Word Current Source is a current regulator circuit which must drive a tightly-controlled pulse of current of over 700 ma through a word line. The pulse should have a rise time of about 100 - 150 nsec, a fall time of 30 - 40 nsec, and a flat top lasting about 100 - 200 nsec as controlled by the input. Current regulation should be within ±5%.

In the past, a word current pulse with a fast leading edge was used in plated wire memories, and the stored information was sensed on that edge. However, the reactive nature of the word line has tended to cause ringing on the leading edge. By sensing information on the trailing edge, a slow leading edge is permissible. This eases the problem of regulation considerably, since overshoot and ringing are eliminated.

To drive current down a word line, first the B- and A-Switch are turned on, in that order (see Technical Report No. 65 for a discussion of these switches.) The Word Current Source is then pulsed. After the Source is turned off at the end of the pulse, the A- and B-Switch are turned off in that sequence. Since the power dissipation in the system is high when word current flows, it is desirable to minimize pulse width variations due, for example, to transistor storage. The Word Current Source was designed with this consideration in mind.

2. CIRCUIT DESCRIPTION

It was decided to use a zener regulator for the Word Current Source. Were a fast rise time required, the relatively long turn-on time of zener diodes would have caused difficulties. The circuit, as yet tentative, is shown in Figure 2-1. It dissipates no standby power. Stages Q1, Q2, and Q3 provide gain, inversion, and level shifting. To minimize transistor storage, stages Q2 and Q3 include anti-saturation diodes D1 - D4. (Note that D1 and D2 are double-junction diodes with high forward drop.) Stage Q4 does not affect circuit operation until the trailing edge of the pulse, and may be ignored for the present. Turning on Q1 causes Q2 and Q3 to turn on. This draws current through the base of Q5 and begins to turn it on. As this happens, the rate of current rise is limited by the inductance of the word line. An increasing voltage developing across R1 is limited when it reaches the breakdown of D7. The breakdown of D7 is selected such that Q5 does not saturate. In this manner, the current flowing through R1 is determined by the zener voltage; and the output

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August 5, 1965

current of the Word Current Source is ($\alpha_5 \times I_{R1}$). Power supply and load impedance variations do not affect regulation.

At the trailing edge of the pulse, Q1, Q2, and Q3 turn off. The negative-going pulse at Q2 turns Q4 on so that the current through R1 is shunted through Q4. This, plus the turn-off of Q5 (aided by the energy stored in L_1), result in a rapid fall of word current.

It was necessary to add diode D10 to protect the circuit against a failure of the +12-v supply or improper voltage sequencing. Without the diode, if the +6-v supply were turned on while the +12-v source were still at ground, base current would flow in Q2 through R4 and R7. When Q2 turned on, Q3 and Q5 would do likewise. The continuous dissipation in components selected for low duty-factor use could cause permanent damage.

Resistor R1 will be selected to provide the optimum word current as determined in tests of the memory. If desirable, a temperature-sensitive resistor can be used either to compensate for the temperature coefficient of the zener diode or to provide a temperature-dependent word current amplitude.

3. PERFORMANCE

Calculations indicate that a current amplitude tolerance of $\pm 4.9\%$ can be held by using this circuit and the A-Switch designed. This figure is the end-of-life tolerance at room temperature. It is assumed that temperature effects will not change with life and can be compensated by R1.

The present circuit provides a rise time of about 125 nsec and fall time of about 30 nsec. There is some overshoot due to the regulation technique which will have to be corrected.

Nominal dissipation has been calculated for the present circuit. Since the width of the word current pulse has not yet been determined, the power is listed as an average value for a maximum information repetition rate (500 KC), per microsecond of word current pulse width.

-3-v	supply:	1.0 mw/usec
+6-v	" :	3.1 mw/usec
+12-v	" :	1.75 mw/usec
+24-v	" :	250 mw/usec

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August 5, 1965

4. REFERENCES

Engineering Notebook #2242 (R. Mosenkis), pp. 31- 32, 35, 36, 58

Technical Report #65, "Word Current Switches and Switch Drivers", R. Mosenkis, August 4, 1965.

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August 5, 1965

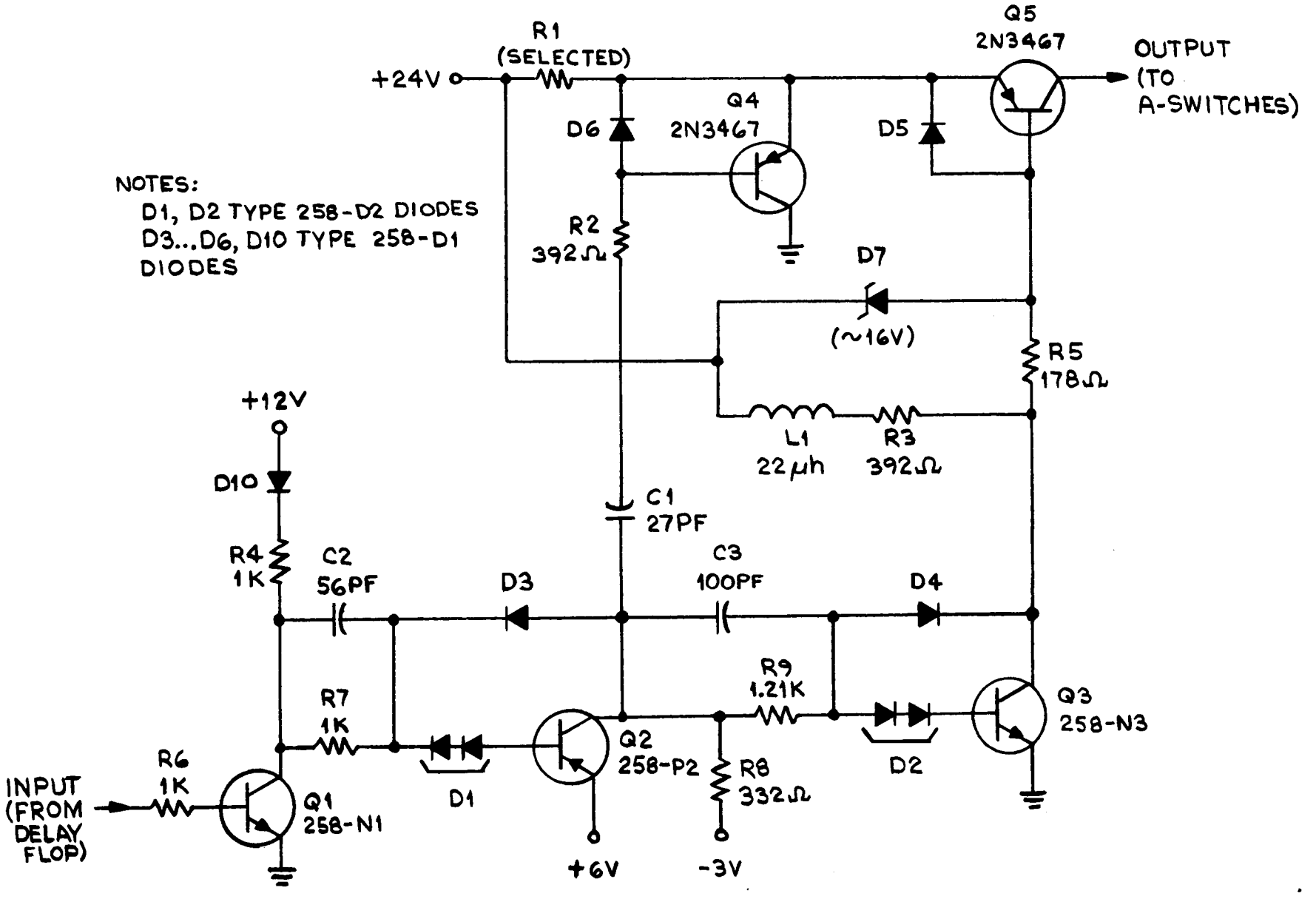

Figure 2-1. Word Current Source Schematic

TECHNICAL REPORT NO. 65

TITLE: WORD CURRENT SWITCHES AND SWITCH DRIVERS

ENGINEER: R. Mosenkis

PROJECT: 258

CONTRACT: NAS 5-9518

UNIT: Advanced Memories

DATE: August 4, 1965

ABSTRACT:

The Word Current Switches and Switch Drivers select one of 2304 word lines in the 1,400,000-bit half-memory. To drive word current down the line, the proper A-Switch and B-Switch are driven by their respective Drivers, then the Word Current Source is pulsed. This report covers the operation of the switches and drivers and discusses their interconnection.

Submitted by: R. Mosenkis
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Approved by: G. A. Fedde
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TECHNICAL REPORT NO. 65

1. INTRODUCTION

In order to select one of the 2304 word lines in the 1,400,000-bit half-memory, a two-dimensional diode matrix is used. The two coordinates of the matrix, labelled A and B, are selected through switches, with the system comprising 24 A-Switches and 96 B-Switches. Since the memory is sequentially addressed, selection of the A- and B-Switches is as follows: One B-Switch is selected, and the 24 A-Switches selected in succession. Then, the next B-Switch is selected together with the 24 A-Switches in succession, etc.

The 24 A-Switches could be selected by means of a 24-stage ring counter, and the 96 B-Switches by a 96-stage ring counter. However, as shown in Figure 1-1, a significant saving in hardware can be effected by use of a 4 x 6 matrix selection of the A-Switch and a 4 x 24 matrix selection of the B-Switch. This requires the addition of four A-Drivers and four B-Drivers (actually, one each of these circuits would have been required anyhow), each one fanning out to six A-Switches or 24 B-Switches, respectively. Selection of an A-Switch is therefore accomplished by ten counter stages and four A-Drivers as opposed to the simple technique of 24 counter stages and one Driver. Matrix selection of the B-Switch cuts the hardware requirement of 96 counter stages and one B-Driver down to 28 counter stages and four Drivers. It was decided to connect only four A- or B-Switches to a counter to minimize capacitive loading on the counter. Were this restriction not imposed, the B selection would have comprised 20 counter stages and eight B-Drivers. The difference is not significant.

In driving word current down a word line, the proper B- and A-Switch are turned on by their respective Drivers. This sends a small current down the word line and charges its capacitance. Then, the Word Current Source is pulsed. In terminating the word current, the sequence is reversed.

2. CIRCUIT DESCRIPTION

2.1 General

A basic understanding of the A- and B-Switches may be gained from Figure 2-1, a simplified diagram. Initially, both Switches were off, and the word lines are reverse-biased to +12 volts. Turning on the B-Switch charges all word lines connected to it to ground potential. When

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base current is supplied to Q1 of the A-Switch, it flows through the matrix diode associated with the selected B-Switch. When the Word Current Source is turned on, its output flows through the collector of Q1 and the matrix diode to the word line and B-Switch. The switching speed of the word current is virtually independent of the switching capabilities of Q1 and Q2, since they are both already on when the Word Current Source is pulsed.

Any noise which appears at the bus joining the 24 word lines common to a B-Switch is capacitively coupled by all 24 lines to the plated wires and degrades the signal-to-noise ratio. This effect is ameliorated by mounting Q2 on the memory plane itself and minimizing the wiring impedance between the word line bus through the B-Switch to ground. Also, the B-Switch has been designed to drive Q2 heavily into saturation, thus minimizing its collector saturation voltage.

2.2 B-Driver and B-Switch

The B-Driver and B-Switch are shown schematically in Figure 2-2. The input to the B-Switch from the Counter is at +12 v when that Switch is not selected and at ground when it is. The input to the B-Driver from its counter turns on Q4 and Q5, causing a positive pulse at the Driver output. This pulse passes through Q3 of the selected B-Switch and turns on Q2. Resistor R2 provides a charging path for the word line capacitance and back-biases the unselected matrix diodes. Diode D1 is required to isolate the capacitance of the four B-Switches connected to each B-Switch Counter from the counter itself. It is expected that the diode be mounted near the counter if significant wiring capacitance will exist between the Switch and the counter.

Initially, R6 was not included in the B-Switch design. However, it was found that a short sneak pulse occurred at a B-Switch output immediately after its counter stage turned off. This was due to the charging, by the B-Driver pulse, of the capacitance in the base circuitry of Q3. Beta multiplication of this charging current through Q3 was sufficient to cause an output at Q2. Resistor R6 to +6 volts serves to charge up this capacitance and prevent the sneak. It also necessitated the addition of diode D2.

2.3 A-Driver and A-Switch

Figure 2-3 comprises a schematic of the A-Switch and A-Driver. Since the base current of Q1 adds to the word current and must, therefore, be well regulated, a zener diode is used in the A-Driver. Selection of the A-Switch by its counter is identical to the B-Switch selection.

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When the A-Driver counter turns Q8 on, it turns on Q7 and breaks down the zener diode, D5. A precise voltage ($V_{D5} - V_{BE7}$) is established across R14 and causes a tightly-controlled current to flow through it. This current, minus base currents of Q6 and Q7 (specified for high beta) and the current into R9, flows into the base of Q1.

Design of the A-Switch is essentially identical to that of the B-Switch. Resistor R1 is necessary as a leakage path for back-biased matrix diodes. Since there are only four A-Drivers in the half-memory, resistor R14 will be selected individually to compensate for initial variations in zener voltages and base voltage of Q7.

3. CIRCUIT SPECIFICATIONS

3.1 General

Since the circuits are quite straight forward, design equations and calculations are not presented here. They may be found in the referenced notebook entries.

Dissipation figures are given for worst case conditions. These include ±4% voltage and ±7% resistor tolerances, except for R14, where ±2% beyond initial tolerance was assumed. The only standby power which is dissipated is that in R6 of the B-Switch and R10 of the A-Switch. There are, at all times, four of each switch connected to a selected counter stage. Dissipation in other circuits exists only when the Driver is pulsed by the counter. Since pulse widths have not yet been finalized, this pulse power is listed per microsecond based on a 500 KC information rate.

The current which must be supplied to the Drivers from the counters and the resultant dissipation is covered in referenced Technical Report No. 64.

3.2 B-Driver and B-Switch

Minimum base current to Q2 . . . . . 100 ma

Maximum dissipation, +6 v (standby, 4 ckts) 0.95 mw total
+12 v . . . . . 25.0 mw/usec

3.3 A-Driver and A-Switch

Minimum base current to Q1 . . . . . 75 ma

Tolerance on I_{word} due to A-Driver and Switch . . . ±11 ma

Maximum dissipation, -3 v . . . . . 18.3 mw/usec
+6 v (standby, 4 ckts) .95 mw total
+12 v . . . . . 20.2 mw/usec

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The word current tolerance listed above is at room temperature, and includes current variations through R_1.

4. REFERENCES

Engineering Notebook 2242 (R. Mosenkis), pp. 39-50

Technical Report #64, "Ring Counter Auxiliary Circuits", R. Mosenkis, July 30, 1965.

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Whitpain
August 4, 1965

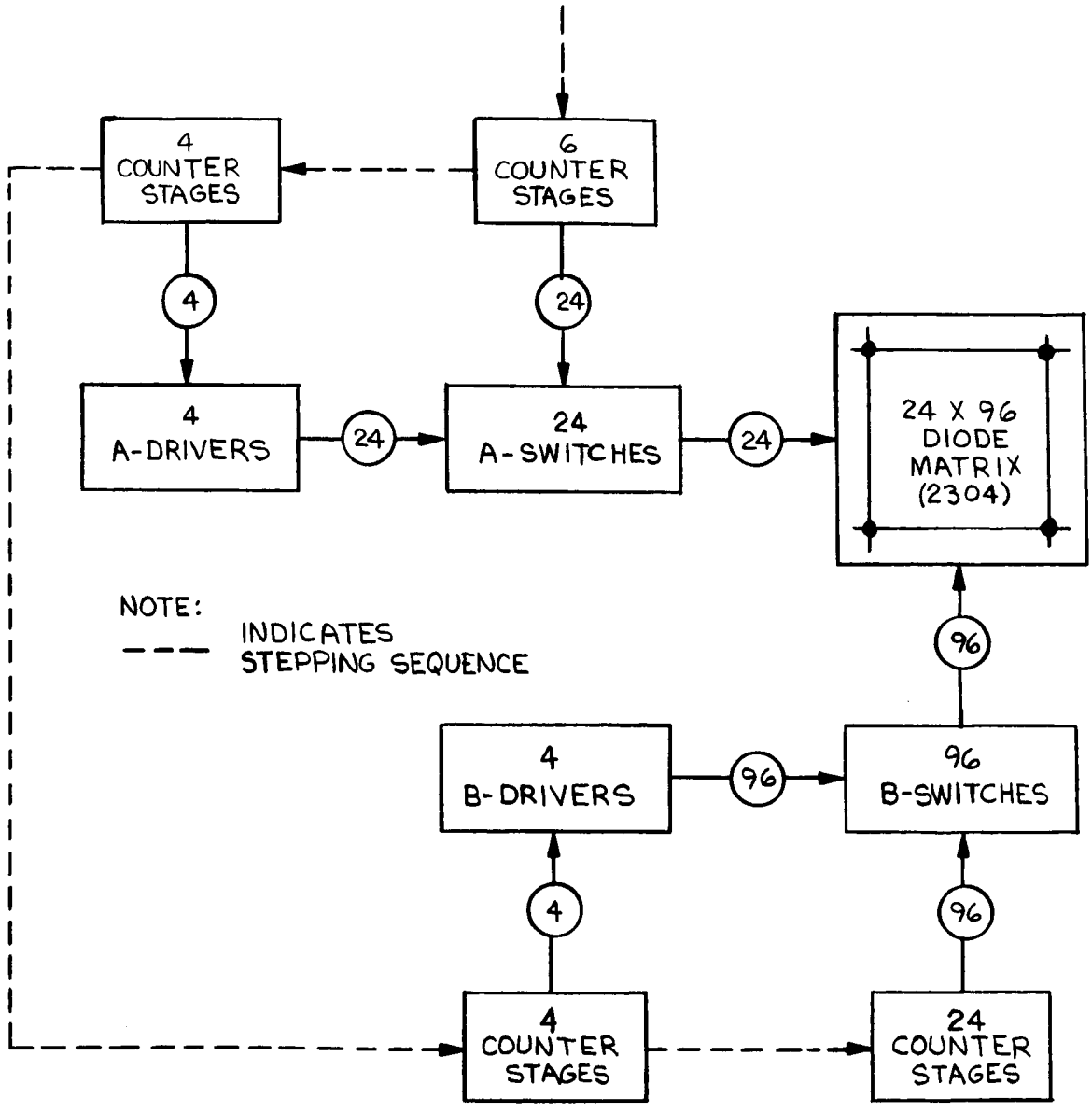

Figure 1-1. Block Diagram Showing Counter Matrixing

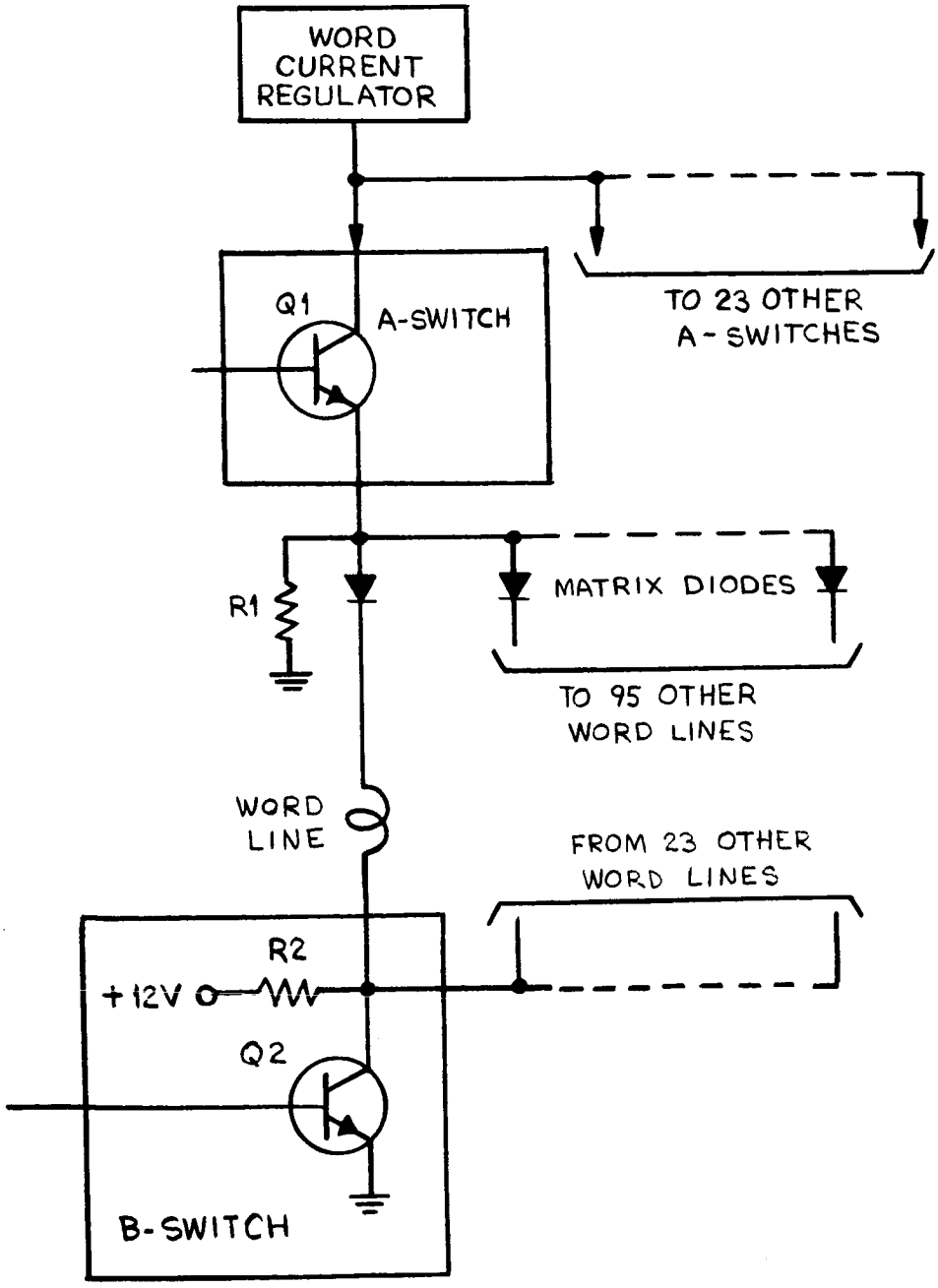

Figure 2-1. Word Current Path

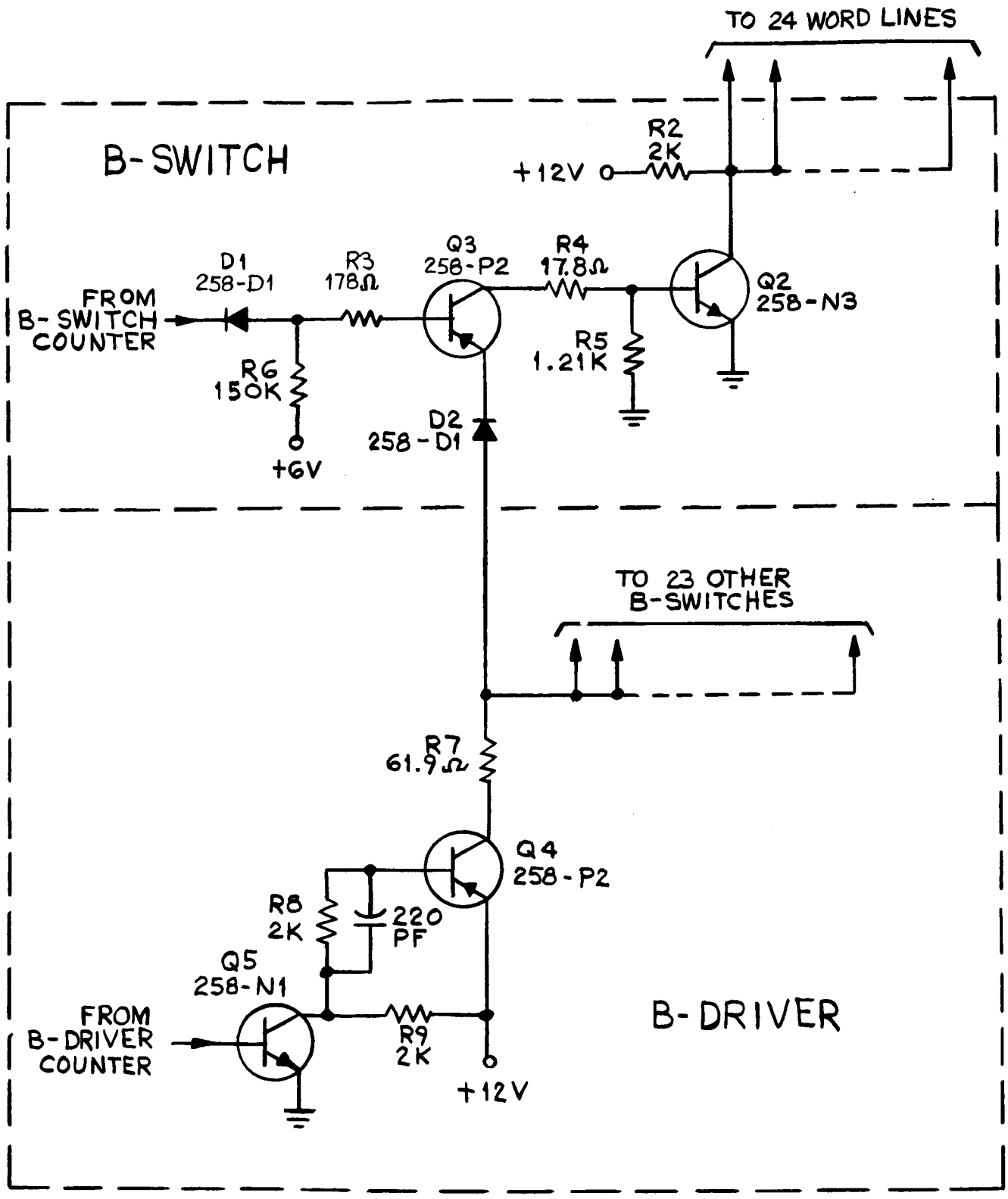

Figure 2-2. B-Driver and B-Switch Schematic

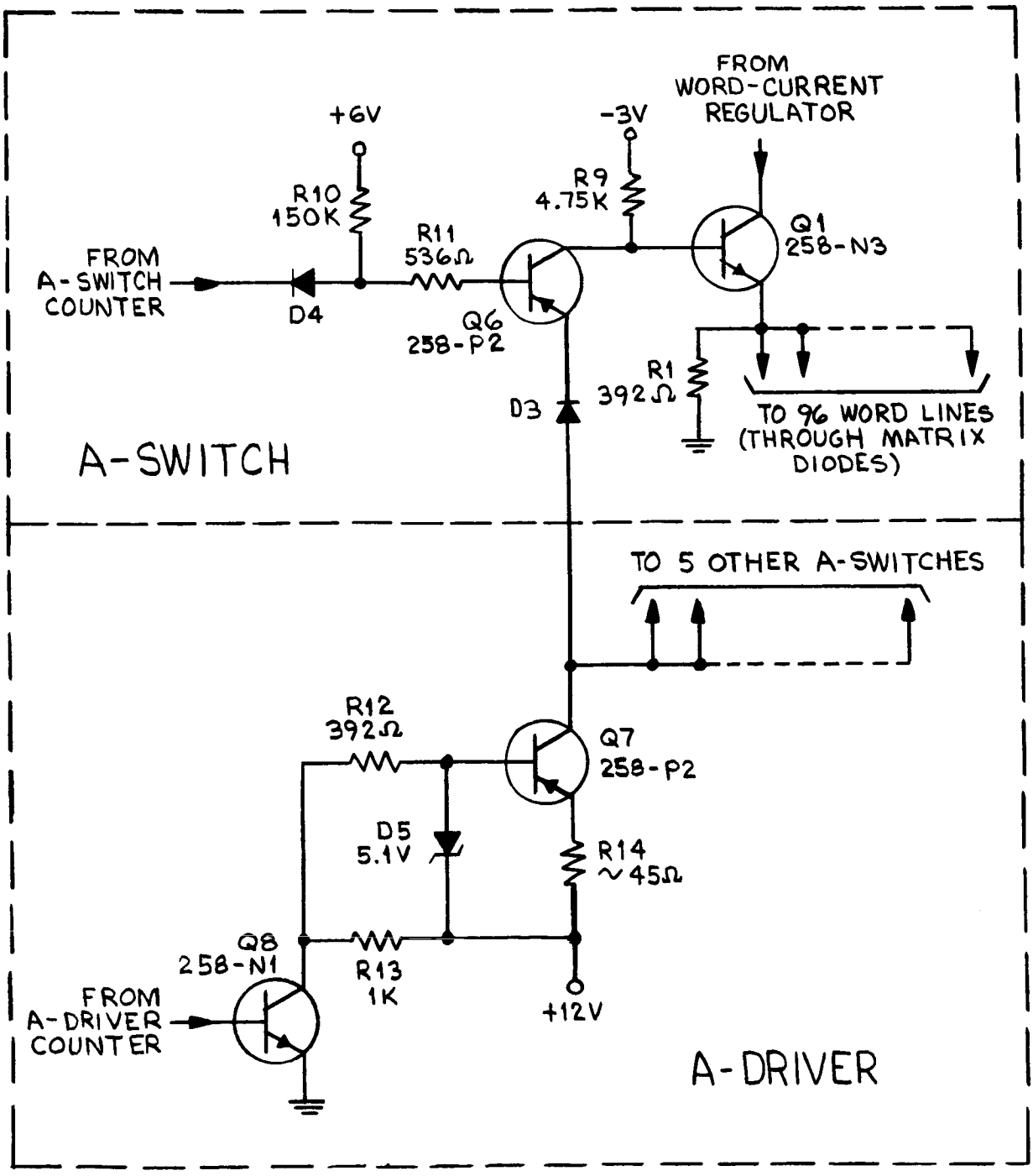

Figure 2-3. A-Driver and A-Switch Schematic

TECHNICAL REPORT # 60

TITLE: Low Power Ring Counter

ENGINEER: R. Mosenkis

PROJECT: 258

CONTRACT: NAS5-9518

UNIT: Advanced Memories

DATE: May 28, 1965

ABSTRACT:

A ring counter for use in address selection is described in this report. Employing complementary transistors, it dissipates a maximum of 6.3 mw in the standby mode, regardless of the number of stages. It is capable of driving heavy loads, when required, by augmenting its input current momentarily. The counter was designed to be stepped every 80 usec or slower.

This report discusses the design and operation of the counter.

Submitted by: R. Mosenkis
R. Mosenkis

Approved by: G. A. Fedde
G. A. Fedde

jam

TECHNICAL REPORT #60

1.0 INTRODUCTION

The counter discussed in this report represents a slight modification of that designed for a previous aerospace contract (NAS5-3171). It is a ring counter whose outstanding feature is low standby power for high drive capabilities. The circuit is insensitive to passive component value changes over a wide range, and therefore lends itself to thin film techniques. It is to be stepped at a maximum rate of 80 usec.

2.0 GENERAL DESCRIPTION OF OPERATION

2.1 Basic Operation

A schematic of several counter stages and their associated circuits is shown in Figure 2-1. To understand its operation, consider the typical counter stage indicated in the figure. Transistors Q_1 and Q_2 form a variation of a silicon controlled rectifier, a device which is usually explained using a two-transistor analogy. The major difference is that a fourth terminal is brought out here. If a positive pulse is applied to the base of Q_2, that transistor will turn on. Current from V_1 may then flow through R_1 and D_1 into the emitter of Q_1. There it will split up into a base and collector current. The collector current serves as base current for Q_2 (except for that part of it which flows into R_4) while its base current flows into the collector of Q_2 (along with I_{R2}). The two transistors thus latch up, and the positive pulse which turned Q_2 on may terminate. Both Q_1 and Q_2 will remain on as long as the holding current, I_{R1}, is not interrupted.

Turning Q_3 on shunts the holding current, I_{R1}, into the collector of Q_3. This leaves Q_1 without emitter current and, hence, Q_2 with no base current. Since Q_2 can no longer accept I_{R2}, its collector rises towards V_1. This positive-going waveform is coupled through C_1 to the base of the Q_2 of the following stage. If Q_3 turns off at this time, I_{R1} is then available to serve as holding current for that stage. Thus, the one stage of the counter which is on propagates down the chain. The only standby power is that caused by I_{R1} and the I_{R2} of one stage, a total of about 6 milliwatts nominally, regardless of the number of stages in the counter. This is in sharp contrast to a ring counter comprised of conventional flip-flops, where each flip-flop dissipates power in both states and the total dissipation is a function of the number of stages.

2.2 High Level Operation

To permit the counter stage to control a high-current load, the holding current I_{R1} is augmented by turning on Q_4 and Q_5. Two types of load are to be driven -- one in which the load current flows into the load and one in which it flows out of the load. Where current is to flow into the load, the load consists of an NPN transistor whose emitter is grounded

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May 28, 1965

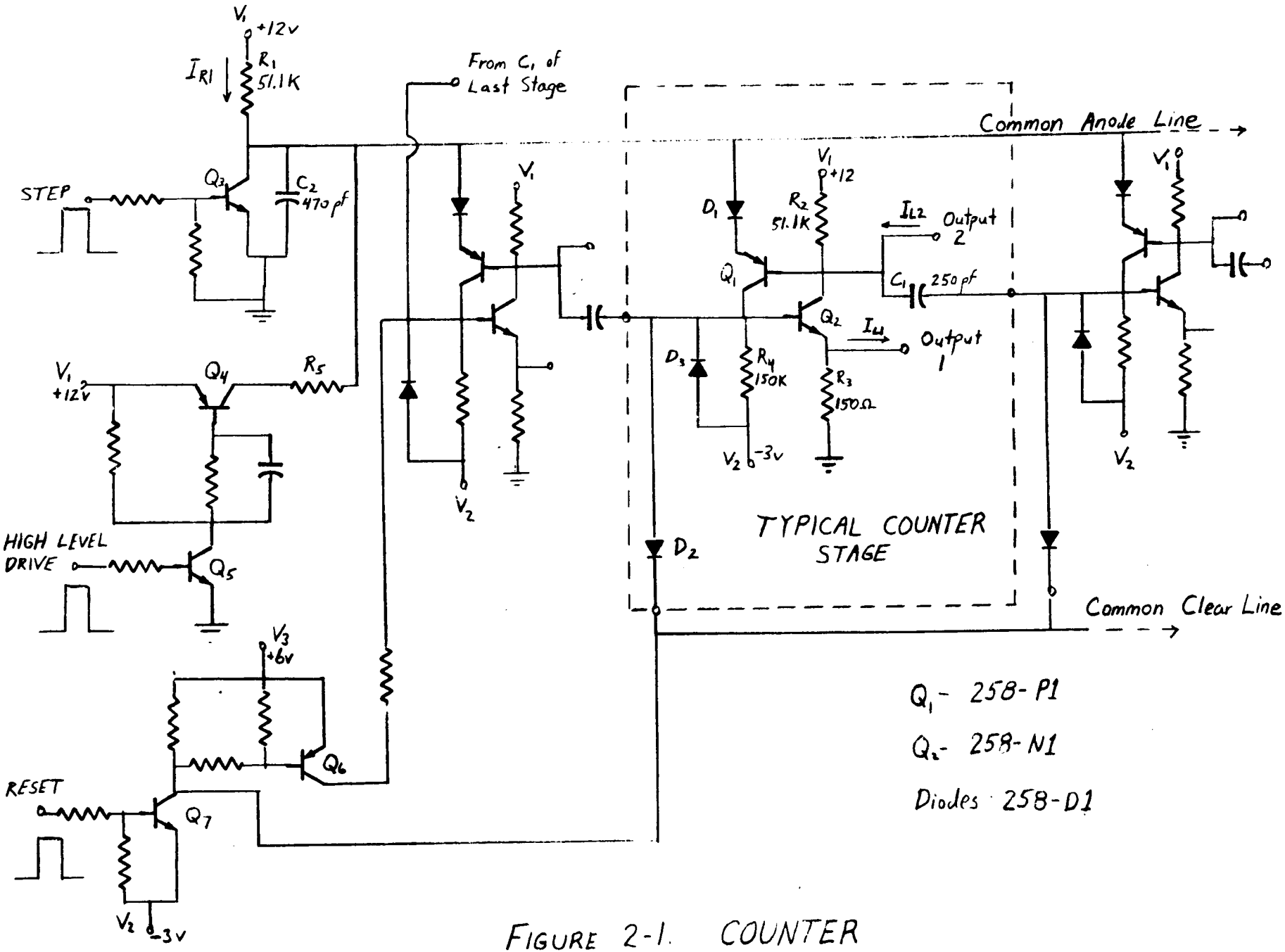

FIGURE 2-1. COUNTER

and whose base is connected across Output 1 of the counter. In the standby condition, the current through R_3 os the ON counter stage is about 0.5 ma. The voltage developed across R_3 is thus some 3.3 millivolts,keeping the load transistor cut off. When the High Level Drive is pulsed on, I_{R5} flows into the Common Anode Line. The only path it finds is through the counter stage which is passing the holding current, I_{R1}. This higher current flows into the emitter of Q_1 and divides in the same manner as did I_{R1} with virtually all of it flowing out of the Q_2 emitter. Sufficient voltage is thus developed across R_3 to turn on the load transistor. The value of R_5 is selected to provide the necessary minimum load current plus the current through R_3 for maximum V_{BE} of the load transistor.

The nature of the load which is applied to Output 2 is somewhat different. Consider a PNP transistor whose emitter is connected to a source of positive-going pulses of amplitude V. If the base of this transistor is connected through a resistor to ground, a common base stage results. A load is connected between the collector and ground. If the base resistor of this PNP were to be connected to a voltage higher than the pulse amplitude V, instead of to ground, the pulses would not be able to pass through it. Thus, the DC voltage to which the base resistor is returned serves as a gate for the pulses. Output 2 of the counter serves as just such a gate. With the base resistor of a PNP just described connected to Output 2 of each counter stage in the string, positive-going pulses are applied to all emitters simultaneously. Only the one transistor connected to the ON counter stage will pass the pulses.

Extending this concept, there is no reason why Output 2 of each counter stage cannot fan out to more than one PNP base resistor. This will permit two-dimensional matrix selection of the PNP. An example will serve to clarify the point. Assume that the counter under consideration consists of ten stages. To Output 2 of each stage are connected (the base resistors of) four PNP's, a total of forty. The emitters of these are brought to four sources of positive pulses such that each source feeds one transistor from each counter stage. Suppose it is desired to drive a different PNP during each successive memory cycle. With the first counter stage ON initially, one of the four pulse sources is energized. During the next memory cycle, the second pulse source is energized; and so on. After the fourth cycle, the counter is stepped and the four pulse sources again energized in turn. In this manner, each of the forty PNP transistors is driven on successive memory cycles. Since the four pulse sources are energized in rotation, they may be controlled by a four-stage counter of this same type. Thus, a total of fourteen rather than forty counter stages is required to select one of forty transistors by means of this two-dimensional matrix.

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In using Output 2 of the counter stage, resistor R_3 is not needed, and is shorted out.

2.3 Resetting the Counter

The counter is reset by simultaneously injecting base current into the Q_2 of the first stage and drawing out the base current of any other stage which might be on. It is possible to reset the counter by a very long step pulse while jamming the first stage ON. This requires an excessive length of time, however, for the following reason: When a step pulse turns a stage off, a positive-going pulse of current is coupled through capacitor C_1 into the base of Q_2 of the following stage, as described previously. This turns on Q_2 of that stage. Since the step pulse is very long, no holding current will flow into that ON stage, and when the capacitively-coupled current ends, that Q_2 will turn off again. The positive-going wave front at its collector will be coupled into the following stage, turning it on momentarily. Thus, there is a relaxation form of ripple through the counter. If the first stage is jammed on, then the ripple-through will end there. The time to reset is then proportional to the number of stages in a counter string. Since the time for a ripple through one stage has been observed at about 25 usec, this form of resetting is not feasible here.

3.0 EQUATIONS AND CALCULATIONS

3.1 General

Where limit (worst-case) equations are shown, the technique of sub- and super-bars will be used to indicate minima and maxima, respectively. These limits apply to the absolute magnitude of the parameter, although the parameter itself is a signed value.

Unless otherwise noted, standard derating factors have been used.

3.2 Standby Operation

The following relationships are evident from an examination of Figure 2-1:

$$I_{E2} = I_{R2} + I_{E1} = I_{R4} \tag{3.1}$$

$$I_{B2} = \frac{I_{E2}}{1 + \beta_2} = \frac{I_{R2} + I_{E1} - I_{R4}}{1 + \beta_2} \tag{3.2}$$

$$I_{B2} = \alpha_1 I_{E1} - I_{R4} \tag{3.3}$$

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The right-hand portions of 3.2 and 3.3 may be equated. Since I_{R4} is almost an order of magnitude less than I_{E1}, little error will be introduced by the approximation $\alpha_1 I_{R4} = I_{R4}$. From this, it is seen that

$$\alpha_1(1 + \beta_2) = 1 + \frac{I_{R2}}{I_{E1} - I_{R4}} \qquad (3.4)$$

From the circuit values, it can be seen that the fractional term in 3.4 is slightly greater than unity. Equation 3.4 gives the current gain requirements for Q_1 and Q_2. If equal demands are to be made of both transistors (i.e., $\beta_1 = \beta_2$), the required beta of each one is equal to the right hand portion of 3.4. (This can be shown by substituting $\beta/(1+\beta)$ for α in the equation.) Thus, a beta of less than 3 is required of Q_1 and Q_2 in standby operation.

3.3 High Level Operation

In this section, the amount of additional current which must be driven into the emitter of Q_1 to drive a required load will be determined.

For a load connected to Output 1, the potential at the base of Q_2 will rise by slightly over 1 volt. The additional current through R_4 caused by this may be neglected. Thus, all the added current I_{E1} will flow through the emitter of Q_2.

$$\Delta I_{E1} = I_{L1} + \Delta I_{R3} \qquad (3.5)$$

From this, it can be seen that

$$\beta_1\beta_2 = 1 \qquad (3.6)$$

a condition which is readily met.

When the load is connected to Output 2, it flows into the collector of Q_2. An increase in I_{E1} is necessary only to provide additional base current to Q_2. It can be seen from Figure 2-1 that neglecting changes in I_{R4},

$$\Delta I_{E1} = \frac{\Delta I_{C2}}{\alpha_1 \beta_2} \qquad (3.7)$$

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The increase in I_{C2} is equal to the load current plus ΔI_{B1}. This second factor is usually negligible.

Use of equation 3.7 is made in the reports concerning the various actual loads.

3.4 Stepping

The stepping of a counter is a rather complex process and is best designed empirically. A complete descriptive analysis of the stepping mechanism is contained in the notebook entries referenced. Suffice it here to state that the changes between the counter used in the previous contract and the one discussed here are minor, and that the reliable operation achieved there is applicable to this project.

4.0 DISSIPATION

The worst-case dissipation in the standby condition will be calculated. This dissipation is due to I_{R1}, I_{R2} and I_{R4}. Assume R_3 shorted to ground.

$$\overline{I_{R1}} = \frac{\overline{V_1} - V_{D1} - V_{CE1} - V_{BE2}}{R_1} \qquad (4.1)$$

Substituting the actual values,

$$\overline{I_{R1}} = \frac{12.48 - .28 - .05 - .35}{.93 \times 51.1} = .25 \text{ ma}$$

$$\overline{I_{R2}} = \frac{\overline{V_1} - V_{CE2}}{R_2} \qquad (4.2)$$

$$= \frac{12.48 - .05}{.93 \times 51.1} = .26 \text{ ma}$$

$$\overline{I_{R4}} = \frac{V_{BE2} - \overline{V_2}}{R_4} \qquad (4.3)$$

$$= \frac{.35 + 3.12}{.93 \times 150} = .025 \text{ ma}$$

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The dissipation is then

$$\overline{P_D} = (\overline{I_{R1}} + \overline{I_{R2}})\,\overline{V_1} + \overline{I_{R4}}\,\left|\overline{V_2}\right| \qquad (4.4)$$

$$= (.25 + .26)\ 12.48 + .025\ (3.12) = 6.33 \text{ mw}$$

5.0 SUMMARY

From the equations of operation derived in Section 3, it can be seen that the steady state operation of the counter -- both in standby and in the high level modes -- makes very little demand upon component values and semiconductor characteristics. Only the stepping can cause difficulties. Since that phase of operation does not lend itself to rigorous analysis, an empirical design was performed. To check this design, the value of the coupling capacitor, nominally 250 pf, was varied from 82 to 820 pf without circuit failure. Also, capacitive loading of Outputs 2 was checked. There is considerable sensitivity to loading at this point, since capacitance will shunt current needed for turning on the next stage. For this reason, the diode necessary to protect the emitter junction of a PNP transistor connected to Output 2 should be mounted near the counter stage. This will isolate the capacitance of the transistor and wiring from the counter. With nominal component values, the counter was operated at a step rate of 26 usec.

6.0 REFERENCES

Engineering Notebook No. 1794, (R. Mosenkis) pp. 72 ff

Engineering Notebook No. 2242 (R. Mosenkis) pp. 1-3, 7-8, 26, 28-30, 33-34

Final Report, Reliable Low-Power Thin-Film Spacecraft Memory (Contract No. NAS5-3171) pp. 118 ff.

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May 28, 1965

TECHNICAL REPORT NO. 64

TITLE: RING COUNTER AUXILIARY CIRCUITS

ENGINEER: R. Mosenkis

PROJECT: 258

CONTRACT: NAS 5-9518

UNIT: Advanced Memories

DATE: July 30, 1965

ABSTRACT:

The Low Power Ring Counter, discussed in Technical Report No. 60, requires several auxiliary circuits for its operation. These are the Stepper, High Level Driver, Reset Circuit and Level Shifter. This report covers the operation of these circuits. Included are a block diagram showing circuit interconnection as well as specifications for each circuit.

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Approved by: G. A. Fedde
G. A. Fedde

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TECHNICAL REPORT NO. 64

1. INTRODUCTION

The Low Power Ring Counter discussed in Technical Report No. 60 employs four auxiliary circuits. These are the Stepper, the High Level Driver, the Reset Circuit, and the Level Shifter. Of these, the first three are required to operate a single ring counter, while the last is used when one ring counter is to be stepped whenever a second counter reaches a predetermined count. This would be done where the two counters form a two-dimensional matrix so that an M-stage counter and an N-stage counter drive (M x N) loads.

A block diagram of two ring counters showing the auxiliary circuits is shown in Figure 1-1.

2. DESCRIPTION OF OPERATION

2.1 Stepper Circuit

The circuit used to step the ring counter is shown in Figure 2-1. Stepping is accomplished by turning on Q1 for about 3 microseconds. For a full description of how this steps the counter, see the Ring Counter report. Capacitor C1 serves two functions; it provides the counter some immunity to noise on the Common Anode Line and it provides a long fall time to the Step pulse. This increases the reliability of the counter.

2.2 High Level Driver

The function of the High Level Driver, shown schematically in Figure 2-2, is to pump additional current into the ON counter stage, thus enabling it to drive a heavier load. In one case where the added current required is small, it was necessary to include R5 to hold Q2 off under worst case conditions. In all other cases, R5 is omitted, the sum of R6 and R7 being sufficient to serve the purpose. The input pulse is derived from a Delay Flop whose output has a 2 K ohm resistor to ground. Holdoff of Q3 is thus ensured.

Five ring counters are used in the memory system, each driving a different load. Coincidentally, two of these loads are nearly identical, so that only four distinct designs were required.

2.3 Reset Circuit

It is desired to reset all ring counters at once. This is accomplished by turning off the ON stage of each counter while jamming the first stage of each counter ON. These two processes are referred

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July 30, 1965

to as Clearing and Setting, respectively. Since the Clear input to each counter stage contains a diode, it is possible to bus them together, and to clear all five counters from a single point. The Set line of the counters must be isolated, though, by diodes in the Reset circuit.

The Reset circuit is shown in Figure 2-3. Since setting a counter requires that current be driven into its first stage, separate resistors are needed to limit the current to each counter. The input to the Reset circuit is derived from a Delay Flop which supplies current at the high (+6 v) level. The input to the Q4 stage is capacitively coupled as a simple expedient for obtaining a level shift. This technique is feasible because Q4 need be on for only a short time.

2.4 Level Shifter

A schematic of the Level Shifter is shown in Figure 2-4. Its input is connected to the output of the last stage of a ring counter, and swings from ground to +12 volts. When that counter stage is ON, the Level Shifter input is at ground, so that Q5 is on, and Q6 off. When the counter stage turns OFF, its output rises to +12 volts, turning Q5 off and Q6 on. The positive-going wavefront at the collector of Q6 triggers the delay flop connected to it, the output of that delay flop generating the Step pulse for the next ring counter. Thus, whenever the last stage of the first counter turns OFF, the second counter is stepped.

The first stage of the Level Shifter was designed to minimize the loading on the counter stage to which it is connected. The second stage provides a low impedance source of trigger current to the delay flop it drives. Of all the counter auxiliary circuits, the Level Shifter is the only one which dissipates power in the standby condition.

3. CIRCUIT SPECIFICATIONS

Presented in tabular form are input and output specifications for the circuits described. These are worst case figures with the input current being the maximum which will be required, and the output current, the minimum which is supplied.

Power dissipation is also included in the figures, broken down between the two power supplies. These figures are worst case, end-of-life. For circuits which do not dissipate any standby power, the figure is given per microsecond of input pulse width, based on a maximum system repetition rate (500 KC). Since the timing of the circuits has not yet been finalized, this is the best form for the power information. Once the pulse width has

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been finalized, it is multiplied by the mw/usec given in the table to yield the average power dissipation. Since the Reset circuit is operated only at the start of a memory command, a time when other circuits are not operated, its average power is truly negligible, and has not been listed. For the Level Shifter, the dissipation is a standby, steady state figure.

All calculations assume ±4% power supply tolerance and ±7% resistor tolerance.

Circuit	Input Current	Output Current	Dissipation +6v	Dissipation +12v
Stepper	0.31 ma	0.26 ma	0.024 mw/usec	(Note 1)
High Level Driver - 1	.22	1.3	.017	.37 mw/usec
- 2	.30	8.6	.24	2.38
- 3	.60	30.0	.47	7.73
- 4	.34	12.6	.27	2.98
Reset	4.5	.50 (set) 2.5 (clear)	Nil	Nil
Level Shifter	.04	.11	1.15 mw	(Note 2)

Notes: 1. Dissipation in R1 included in Ring Counter.

2. Standby power. All others are per microsecond pulse width.

4. REFERENCES

Since all circuits described in this report are of a very simple nature, calculations have not been included here. The following notebook references contain all pertinent calculations and derivations:

Engineering Notebook #1794 (R. Mosenkis), p. 72
Engineering Notebook #2242 (R. Mosenkis), pp. 26, 33, 51-57, 59-60.

Also pertinent is Technical Report No. 60, "Low Power Ring Counter." R. Mosenkis, May 28, 1965.

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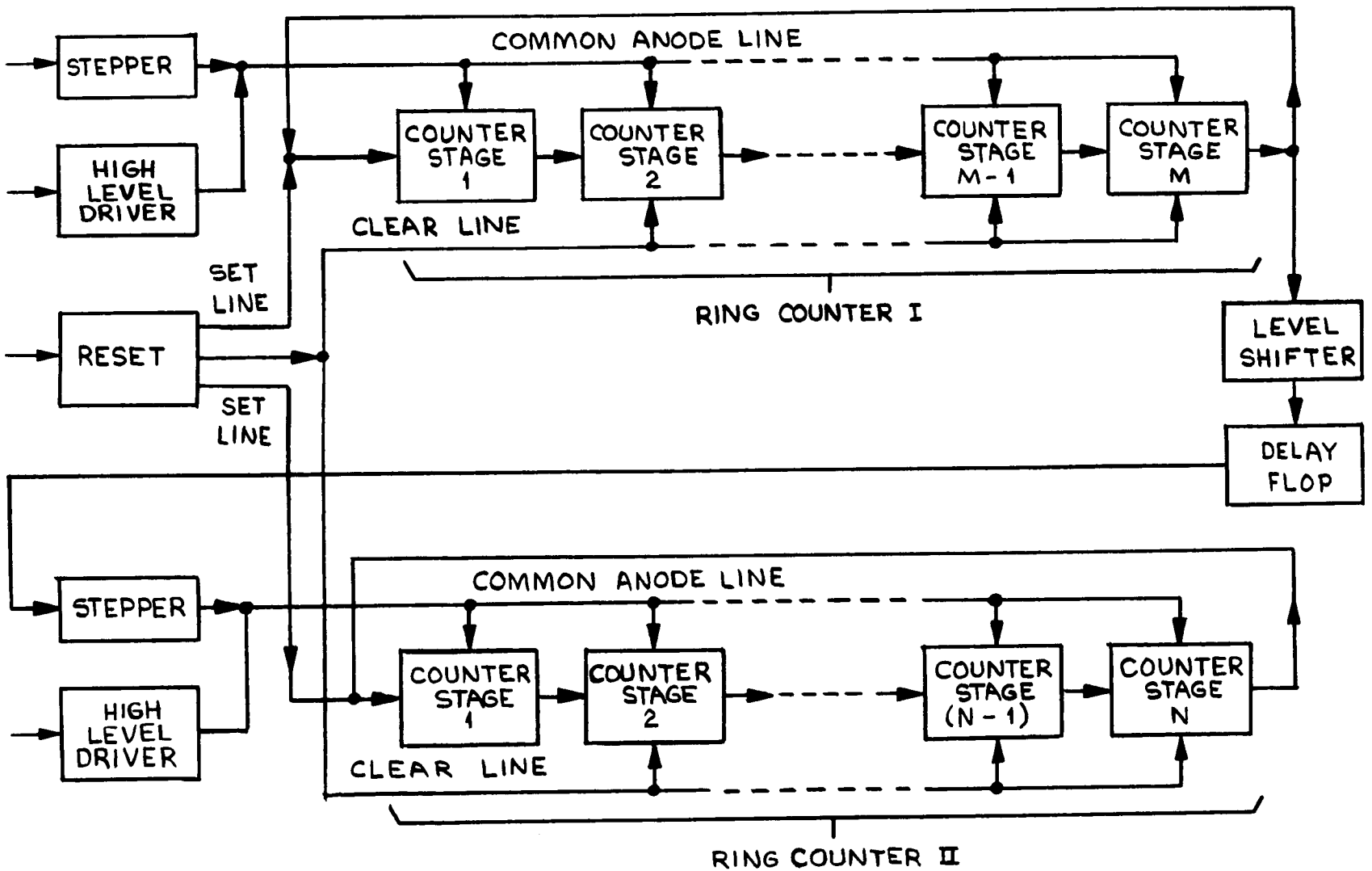
July 30, 1965



NOTE:
LOADS NOT SHOWN ON COUNTER STAGES

Figure 1-1. Block Diagram

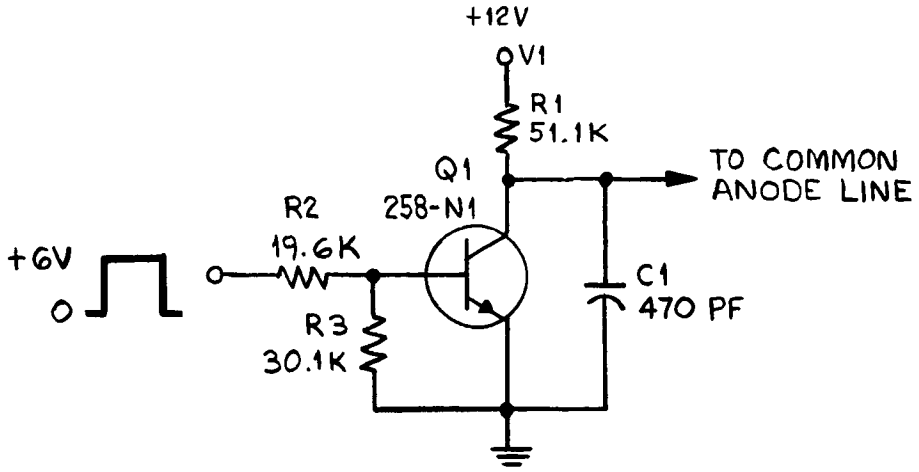
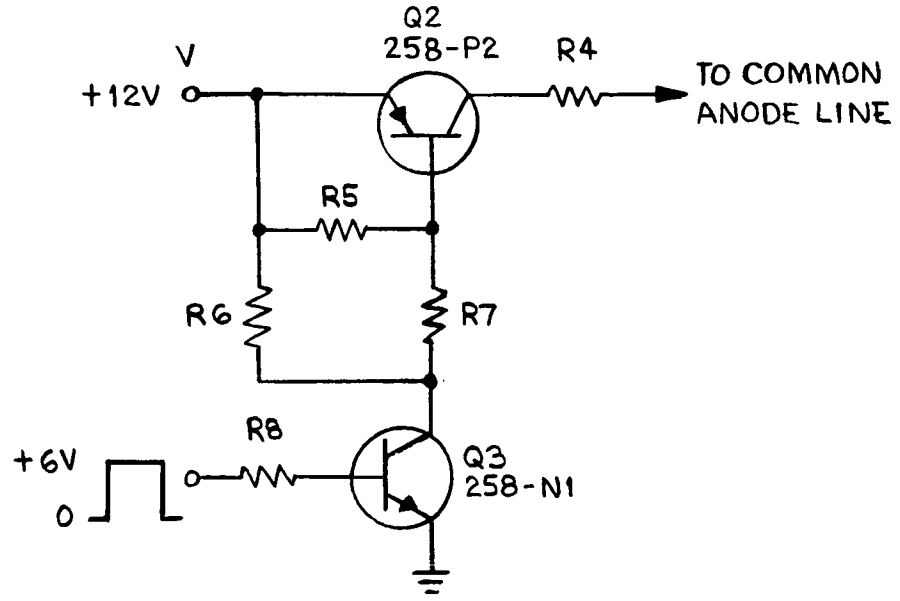


Figure 2-1. Ring Counter Stepper



VARIATION	R4	R5	R6	R7	R8
1	6.49K	30.1K	10K	90.9K	27.4K
2	825Ω	-	10K	22.1K	20K
3	221Ω	-	10K	4.64K	10K
4	562Ω	-	10K	14K	17.8K

Figure 2-2 High-Level Driver

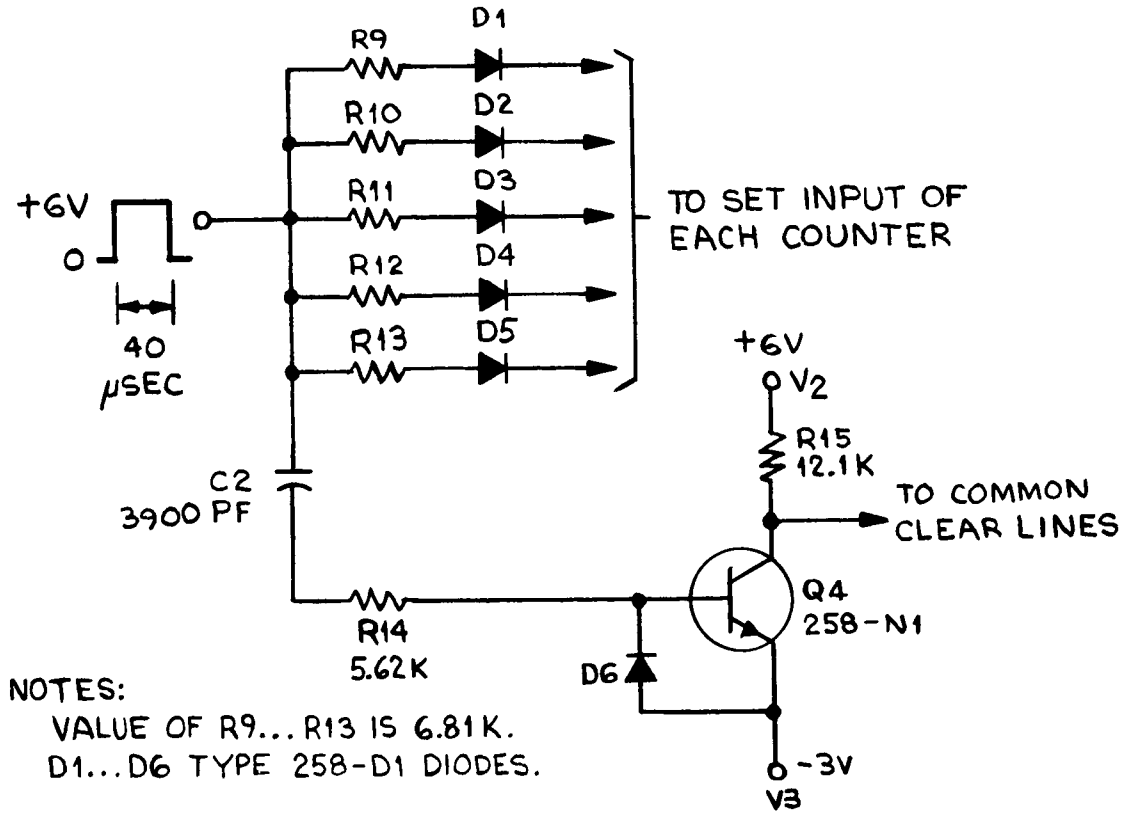


Figure 2-3. Ring Counter Reset Circuit

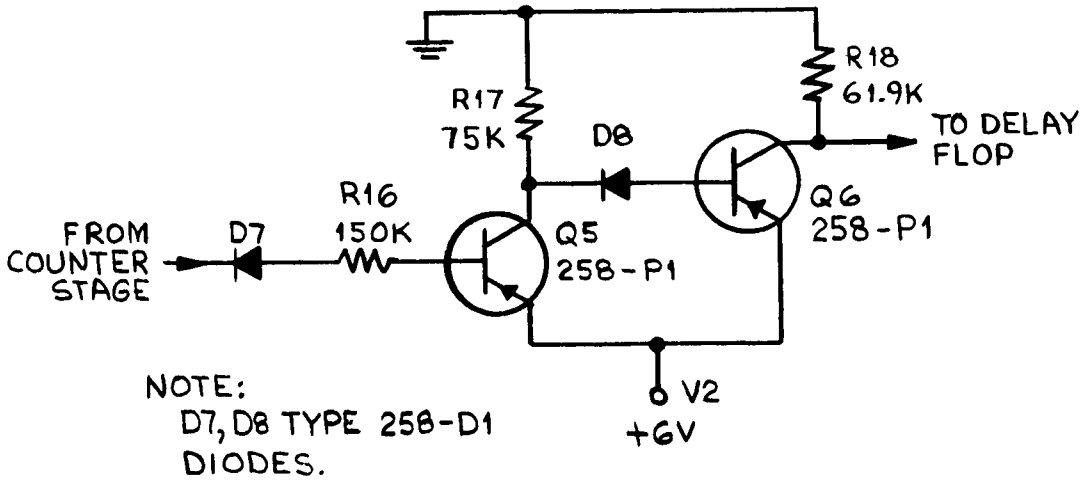


Figure 2-4. Ring Counter Level Shifter

APPENDIX II

COMPONENT PARTS LIST

CIRCUIT LIST

Contract No. NAS5-9518

Type	Drawing No.	No. Required	Thin Film Circuit Type
Buffer Register	R58-001	4	
Counter Inverter	-002	4	
Counter Pulser	-003	28	
Pulse Amplifier	-004	5	
Pulse Gate	-005	14	
Information Counter	-006	14	
Information Counter Stepper	-007	2	
Output Buffer	-008	1	
Output Flip-Flop	-009	1	
Logic Inverter	-010	2	
Logic Gate	-011	2	
Pause Flip-Flop	-012	1	
Delay Flop	-014	20	
Differential Amplifier	-015-A	40	P-HC-06-1
Read Amplifier Output	-015-B	40	P-HC-06-2
Bit Driver	-016-A	40	P-HC-02
Bit Driver Output	-016-B	40	
Bit-Sense Matrix	-017	140	P-HC-03
Information Register	-018	40	P-HC-04
Ring Counter	-019	27	P-HC-05
B-Switch	-020	96	
B-Switch Driver	-021	4	
A-Switch	-022	24	
A-Switch Driver	-023	4	
Word Current Source	-024	1	
Ring Counter Stepper	-025	5	
Ring Counter High Level Driver	-026	5	
Ring Counter Reset	-027	1	
Ring Counter Level Shifter	-028	4	
Bit-Sense Matrix Driver	-029-A	16	
Dummy Matrix Driver	-029-B	2	
Bit Timing Pulser	-030	1	
Bit Power Pulser	-031	1	
Read Gate Pulser	-032	1	

PARTS LIST

Contract NAS5-9518

ACTIVE COMPONENTS

None of the active components listed in the attached Tables are listed on the GSFC preferred parts list.

PASSIVE COMPONENTS

All of the listed passive components are on the GSFC preferred parts list.

Submitted: 6/29/65

TRANSISTORS

Type	Total	Mfg.	Mfg. Type	Maximum Specified Rating		Maximum Applied Stress
258-N1	351	Motorola	2N2501	BV_{CBO}	40V	12V
				BV_{EBO}	6V	3V
				P_D @ 80°C	250 mw	6 mw
258-N2	201	Motorola	2N3493	BV_{CBO}	12V	4V
				P_D @ 80°C	100 mw	0.6 mw
258-N3	16	Fairchild	2N3302	BV_{CBO}	60V	24V
				BV_{EBO}	5V	3V
				P_D @ 80°C	250 mw	11mw
258-N4	96	Fairchild	2N3302 (TO-46)	BV_{CES}	30V	12V
258-P1	12	Motorola	2N3251	BV_{CBO}	40V	12V
				BV_{EBO}	5.6V	3V
				P_D @ 80°C	250 mw	1.0mw
258-P2	103	Fairchild	2N3504	BV_{CEO} (Sust.)	45V	12V
				BV_{EBO}	5.0V	1.0V
				P_D @ 80°C	280mw	1.0mw
258-P_3	75	Fairchild	2N2894	BV_{CBO}	12V	6V
				P_D @ 80°C	250 mw	1.0mw
258-P4	61	Fairchild	2N3209	BV_{CBO}	20V	12V
				P_D @ 80°C	250mw	1.0mw
258-C1	840	Motorola	SL-1	BV_{EBO}	6.0V	3V
				P_D @ 80°C	100mw	.05mw
258-C2	840	Motorola	SL-45	BV_{EBO}	5.5V	3V
				P_D @ 80°C	100 mw	.05mw

DIODES

Type	Total	Mfg.	Mfg. Type	Maximum Specified Rating		Maximum Applied Stress
258-D1	1500	Micro-Semiconductor	1N3207	BV @ 100 ua.	60V	12V
				P_D @ 80°C	140mw	1.0mw
258-D2	138	General Electric	1N4156	BV	20V	3V
				P_D @ 80°C	280mw	0.5mw
258-D3	28	General Electric	1N4453	BV	20V	6.0V
				P_D @ 80°C	280mw	0.3mw
258-D4		Motorola	1N751A (Zener)	BV	5.85V	5.85V
				P_D @ 80°C	250mw	0.5mw

RESISTORS

Type	Total	Mfg.	Mfg. Type	Maximum Specified Rating	Maximum Applied Stress
CHM-5	1245	Electra	CHM-5	1/8 watt @ 125°C	10mw
Thin Film	1322	CTS	Cermet	P 25 mw @ 80°C	1.0mw
Thin Film	2520	Halex	Nichrome	P 5mw @ 80°C	1.0mw

CAPACITORS

Type	Total	Mfg.	Mfg. Type	Maximum Specified Ratings	Maximum Applied Stress
Glass	239	Corning	CYFR-10	500V	24V
Ceramic	5	Vitramon	VK	200V	15V
Tantalum	18	Sprague	350D	20V	12V
Thin Film	414	CTS	Ceramic Chip	25V	

TRANSFORMERS

Type	Total	Mfg.	Mfg. Type	Maximum Specified Ratings	Maximum Applied Ratings
258-T1	40	UNIVAC	258-T1	300VDC	12V
258-T2	18	UNIVAC	258-T2	300VDC	12V
Inductor	1	Delevan	1537	250V	24VAC

APPENDIX III

SPECIFICATIONS FOR HYBRID CIRCUITS AND SEMICONDUCTORS

P-HC-02

REVISIONS					
ZONE	E.I.R.	DESCRIPTION	DATE	CHK'D	APP'D
—			4-15 6.5		

P-HC-02

BIT DRIVER

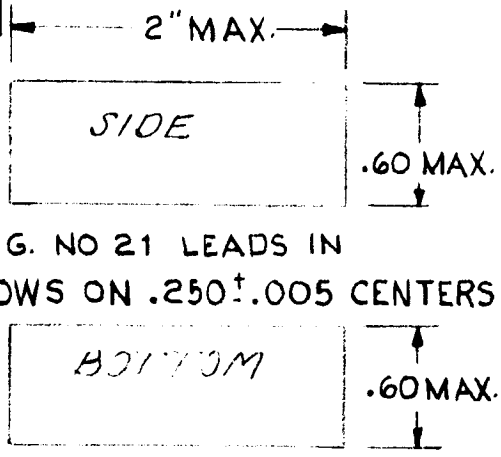
PROJECT 258

		CLASS	UNIVAC
			PURCHASED PART DRAWING
		TYPE	
		TITLE	CIRCUIT, INTEGRATED, HYBRID (BIT DRIVER)
		CODE IDENT NO.	SIZE: A — DWG NO: P-HC-02
		CATALOG CODE	SHEET 1 OF 4

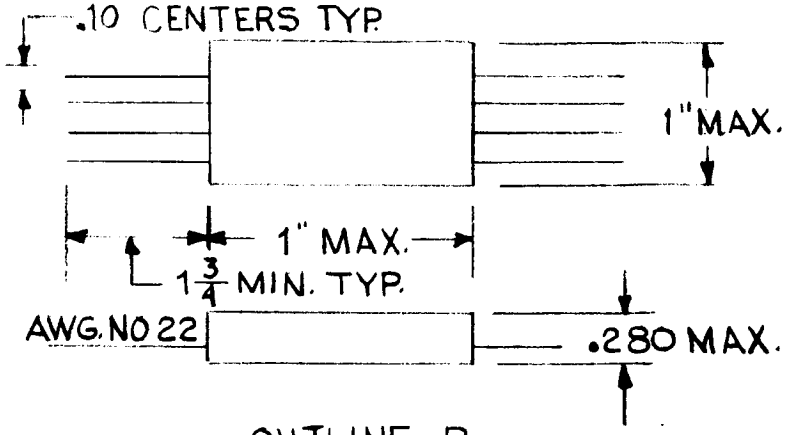
UNLESS OTHERWISE SPECIFIED: ALL DIMENSIONS ARE IN INCHES. TOLERANCE ON FRACTIONS | DECIMALS | ANGLES

DWG. NO. P-HC-02

MECHANICAL OUTLINE
(A OR B ACCEPTABLE)

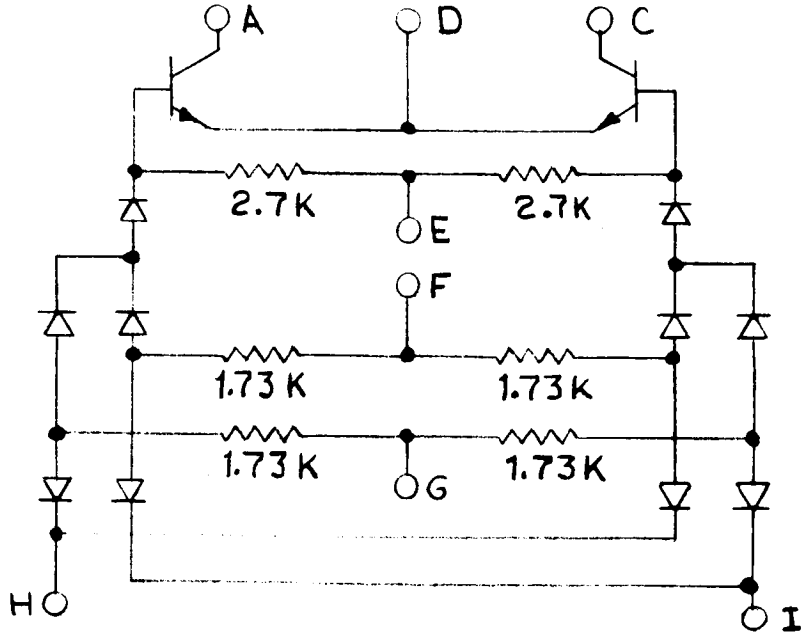


OUTLINE A



OUTLINE B

SCHEMATIC
BIT DRIVER



UNIVAC

CIRCUIT, INTEGRATED,
HYBRID (BIT DRIVER)

SIZE A | DWG NO. P-HC-02

SHEET 2 OF 4

REVISIONS

ZONE	E/O	DESCRIPTION	DATE	BY	APPD

REQUIREMENTS:

GENERAL: HYBRID INTEGRATED CIRCUIT (BIT DRIVER)

PHYSICAL:

CONSTRUCTION: CONFORMAL EPOXY COATED OR EPOXY-FILLED PRE-MOLDED PLASTIC CASE

MARKINGS: UNIVAC PART NO., LEAD IDENTITY, EIA DATE CODE AND VENDOR IDENTIFICATION ON TOP OF UNIT

TERMINALS: TINNED COPPER

TERMINAL STRENGTH: PER MIL-STD-202C, METHOD 211, CONDITION A (3 LBS.) AND CONDITION D

ELECTRICAL: (AT 25 $\pm 2^{\circ}$C AMBIENT):

TRANSISTORS: PER 258-N1

DIODES: PER 258-D1

RESISTORS:

D.C. RESISTANCE: SEE SCHEMATIC

RESISTANCE TOLERANCE: $\pm 1\%$

TEMPERATURE COEFFICIENT (BETWEEN -20°C AND $+80^{\circ}$C): ± 350 PPM/$^{\circ}$C MAX.

POWER RATING AT 80°C, AS ENCAPSULATED: 25 MW PER RESISTOR

MODULE: INSULATION RESISTANCE, ANY PIN TO CASE AT 100V DC 50K MEG OHMS

ENVIRONMENTAL:

OPERATING TEMPERATURE RANGE: -20°C TO $+80^{\circ}$C

STORAGE TEMPERATURE RANGE (48 HOURS): $+150^{\circ}$C

RELATIVE HUMIDITY: 100% R.H., INCLUDING FROST OR WATER CONDENSATION.

TEMPERATURE CYCLING: MUST MEET REQUIREMENTS OF MIL-STD-202, METHOD 107A, CONDITION A (EXCEPTION: $\leq$ 1 MINUTE BETWEEN TEMPERATURE EXTREMES). TEST PER TEST SPECIFICATION.

UNIVAC

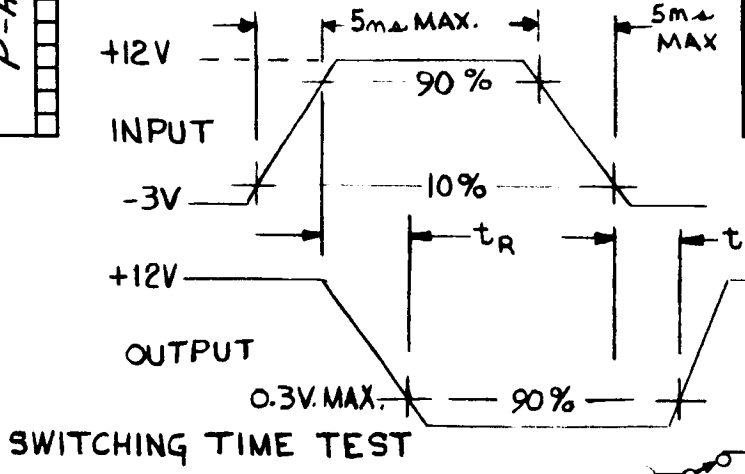
CIRCUIT, INTEGRATED, HYBRID (BIT DRIVER)

SIZE A | P-HC-02

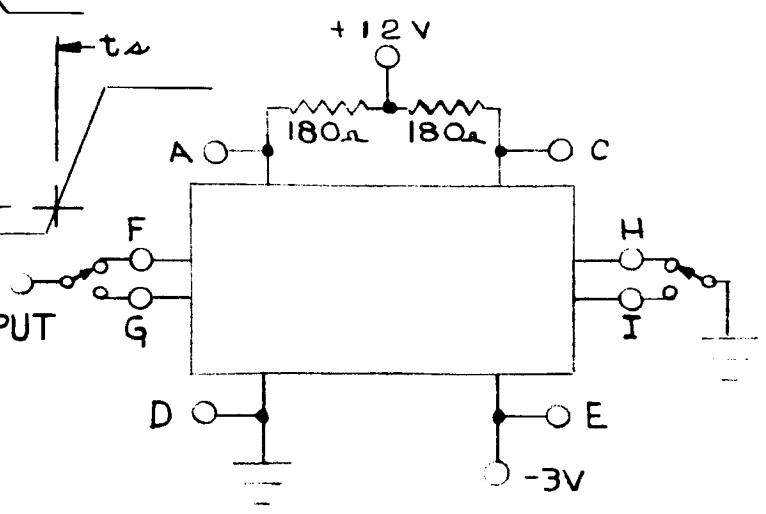
SHEET 3 OF 4

P-HC-02

ELECTRICAL TEST SPECIFICATIONS
(AT 25 ± 2° C)



SWITCHING TIME TEST



POINT IN	POINT GND	POINT OUT	
F	H	A	$t_r \leq 35$ ns
F	I	C	
G	H	C	$t_s \leq 40$ ns
G	I	A	

Leakage Current Test

With terminals F, G, H, and I open, 12 volts applied to terminals A and C, -3 volts applied to terminal E, and terminal D grounded, the current flowing from terminal E shall not exceed 50 na.

UNIVAC

CIRCUIT, INTEGRATED, HYBRID (BIT DRIVER)

A P-HC-02

SHEET 4 OF 4

P-HC-03

REVISIONS					
LTR	ECR	DESCRIPTION	DATE	DRN	APVD
—			4-15-65		

P-HC-03

BIT SENSE MATRIX

PROJECT 258

R.G. [illegible]	4/15/65	UNIVAC	
C.A. [illegible]	4/15/65	PURCHASED PART DRAWING	
		TYPE	
		TITLE: CIRCUIT, INTEGRATED, HYBRID (BIT SENSE MATRIX)	
		CODE IDENT NO. A	SIZE / DWG NO. P-HC-03
			SHEET 1 OF 5

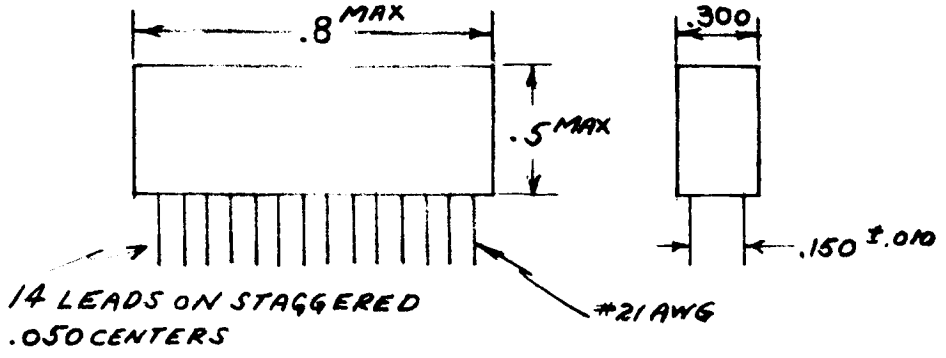
TTT-5

P-HC-03

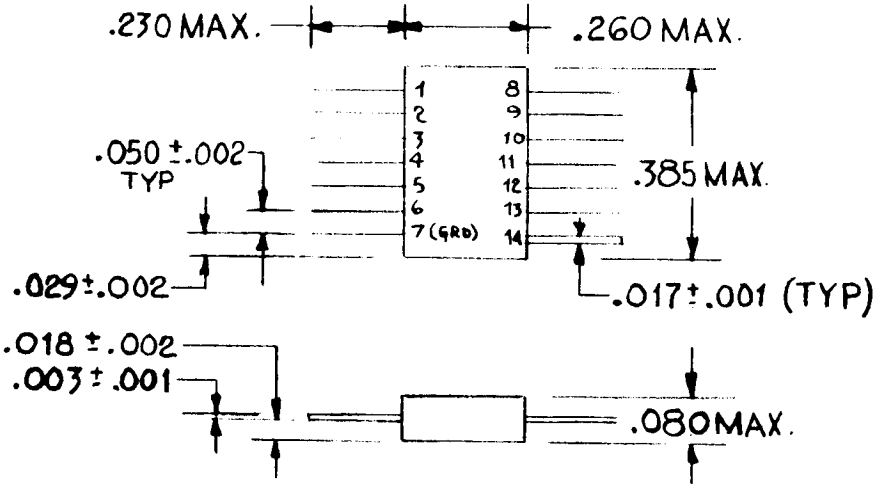
REVISIONS

ZONE	LTR	DESCRIPTION	DATE	CHK	APPD

MECHANICAL OPTION A



MECHANICAL OPTION B



UNIVAC

TITLE: CIRCUIT, INTEGRATED HYBRID (BIT SENSE MATRIX)

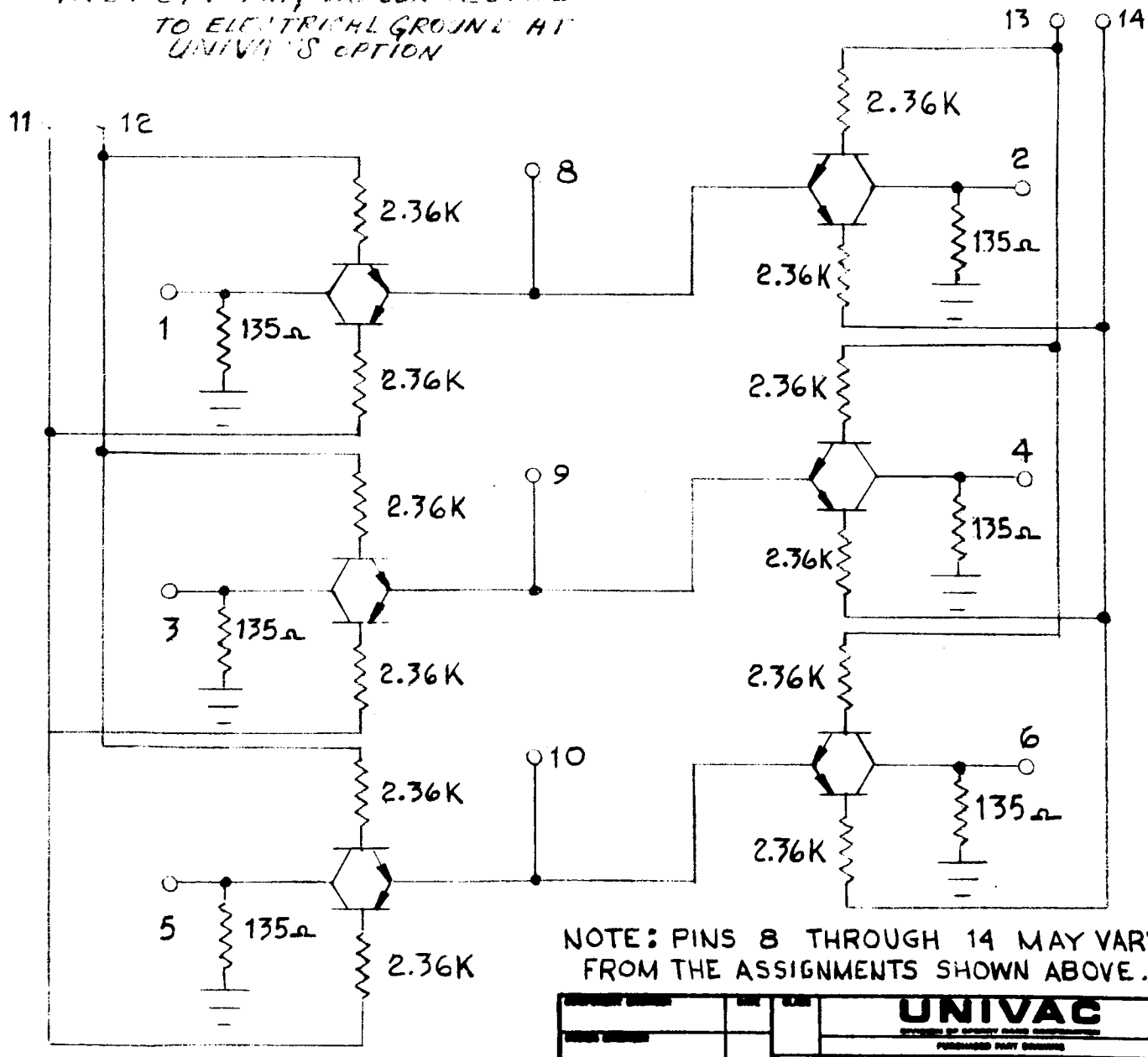
SIZE A | DWG NO. P-HC-03

SHEET 2 OF 3

P-HC-03

SCHEMATIC

NOTE: CASE MAY BE CONNECTED TO ELECTRICAL GROUND AT UNIVAC'S OPTION



NOTE: PINS 8 THROUGH 14 MAY VARY FROM THE ASSIGNMENTS SHOWN ABOVE.

UNIVAC

CIRCUIT, INTEGRATED, HYBRID (BIT SENSE MATRIX)

A P-HC-03

SHEET 3 OF 5

JA

ITT-7

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	CHK'D	APP'D

Requirements:
General: Hybrid Integrated Circuit (Bit Sense Matrix)
Physical:
Construction:
Mechanical Option A: Epoxy-Filled Pre-Molded Plastic Case
Mechanical Option B: Hermetically-Sealed Gold Plated Kovar Case

Markings: UNIVAC Part No., Lead Identity, EIA Date Code, And Vendor Identification On Top Of Unit
Terminals:
Mechanical Option A: Tinned Copper
Mechanical Option B: Gold Plated Kovar Leads
Terminal Strength: (Mechanical Option A Only) Must Meet MIL-STD-202C, Method 211, Condition A (3 Lbs.) and Condition D.

Electrical (At 25°C +2°C Ambient):
Transistors: Per 258-C1 (NPN; Per 258-C2 (PNP)
Resistors:
D. C. Resistance: (See Schematic)
Resistance Tolerance: +1%
Max. Temperature Coefficient (Between -20°C And +80°C):
±350 PPM/°C; (2.36K Ohms Units Matched To ±50 PPM/°C Max.)
Min. Power Rating At 80°C, As Encapsulated: 25 MW Per Resistor
Insulation Resistance, Any Pin To Case At 100 VDC: 50K Meg Ohms Min.

Environmental:
Operating Temperature Range: -20°C To +80°C
Storage Temperature Range: (48 Hours) +150°C
Relative Humidity: 100% RH, Including Frost Or Water Condensation
Temperature Cycling: Must Meet Requirements Of MIL-STD-202, Method 107A, Condition A (Exception: ≤ 1 Minute Between Temperature Extremes). Test Per Test Specification.

UNIVAC
DIVISION OF SPERRY RAND CORPORATION
PURCHASED PART DRAWING

TYPE
TITLE CIRCUIT, INTEGRATED, HYBRID (BIT SENSE MATRIX)

SIZE A | DWG NO. P-HC-03

SHEET 4 OF 5

REVISIONS

SYM	ECR	DESCRIPTION	DATE	CHK	APPD

ELECTRICAL TEST SPECIFICATIONS:

THE TERMINAL NUMBERS CORRESPOND TO THOSE SHOWN IN THE SCHEMATIC.

I. LEAKAGE CURRENT TEST

GROUND TERMINALS 1 THRU 10

A) APPLY +3 VOLTS TO TERMINALS 11 AND 14. THE SUPPLY CURRENT SHALL NOT EXCEED 180 NADC.
B) APPLY -3 VOLTS TO TERMINALS 12 AND 13. THE SUPPLY CURRENT SHALL NOT EXCEED 180 NADC.

II. LARGE CURRENT SATURATION TEST

GROUND TERMINALS 1 THRU 7

A) APPLY +6 VOLTS TO TERMINAL 12 AND -6 VOLTS TO TERMINAL 11. TERMINALS 13 AND 14 ARE FLOATING. WITH $\pm$30 MA DC CURRENT APPLIED TO TERMINALS 8, 9 OR 10, THE VOLTAGE AT TERMINALS 8, 9, OR 10 SHALL NOT EXCEED $\pm$0.35 VOLTS.
B) REPEAT II (A) WITH +6 VOLTS APPLIED TO TERMINAL 13, -6 VOLTS APPLIED TO TERMINAL 14, AND WITH TERMINALS 11 AND 12 FLOATING

III. SMALL SIGNAL RESISTANCE TEST

GROUND TERMINALS 1 THRU 7

A) APPLY +6 VOLTS TO TERMINAL 12 AND -6 VOLTS TO TERMINAL 11. TERMINALS 13 AND 14 ARE FLOATING. WITH A SMALL SIGNAL CURRENT ($\leq$ 100μA) FLOWING BETWEEN TERMINAL 8, 9 OR 10 AND GROUND, THE SMALL SIGNAL RESISTANCE BETWEEN TERMINAL 8, 9, OR 10 AND GROUND SHALL NOT EXCEED 15 OHM.
B) REPEAT III (A) WITH +6 VOLTS APPLIED TO TERMINAL 13, -6 VOLTS TO TERMINAL 14, AND WITH TERMINALS 11 AND 12 FLOATING.

NOTE: UNIVAC WILL SUPPLY A TEST FIXTURE FOR TEST III AT THE MANUFACTURERS OPTION.

UNIVAC
DIVISION OF SPERRY RAND CORPORATION
PURCHASED PART DRAWING

TYPE
TITLE CIRCUIT, INTEGRATED, HYBRID (BIT SENSE MATRIX)

CODE IDENT NO. | SIZE A | DWG NO. P-HC-03
CATALOG CODE | SHEET 5 OF 5

DWG. NO. P-HC-04

REVISIONS					
DWG	ECR	DESCRIPTION	DATE	CHK.	APPD
A		REVISION ON SH. 6	1-8		
B		REVISED SHTS 2 & 4	2-3-65		

P-HC-04

FLIP FLOP

PROJECT 258

SHEET INDEX	SH.	1	2	3	4	5	6
	REV.	B	A	—	A	—	A

UNIVAC

CIRCUIT, INTEGRATED, HYBRID (FLIP FLOP)

SIZE A | DWG NO. P-HC-04

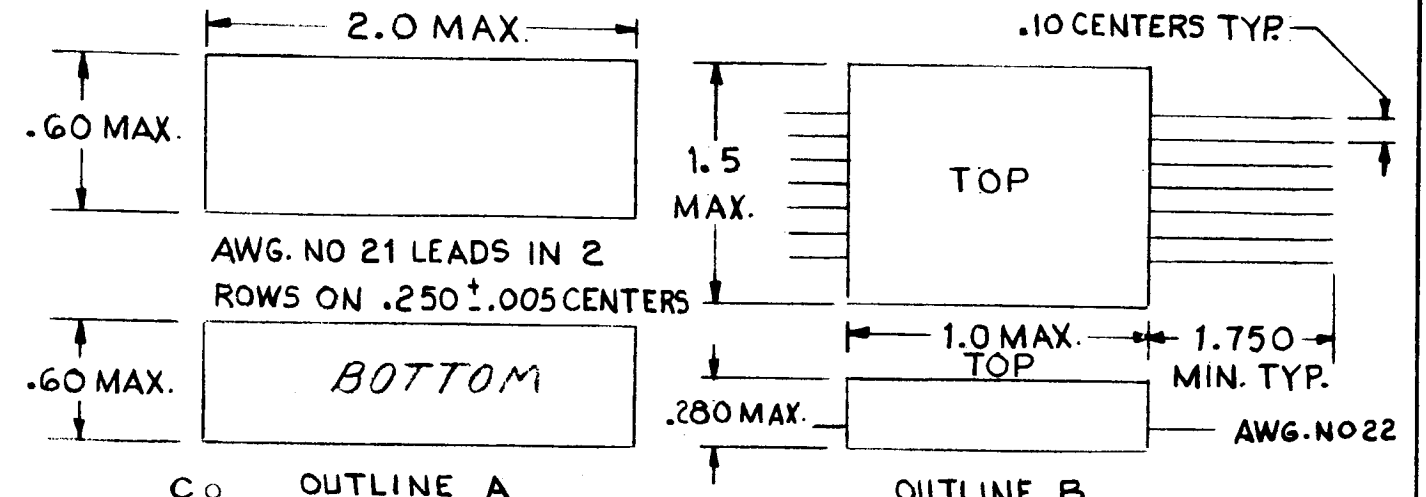
SHEET 1 OF 6

P-HC-04

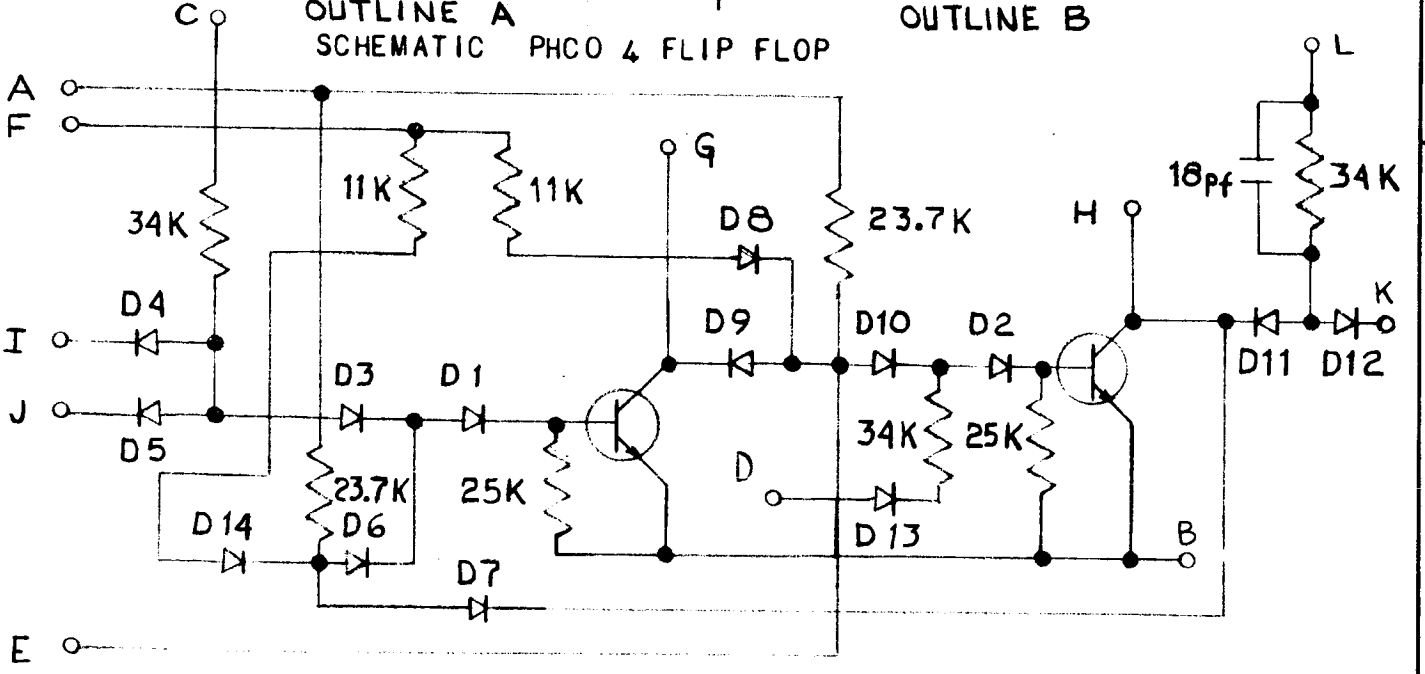
MECHANICAL OUTLINE

A OR B ACCEPTABLE

—			7-28		
A		REM C-L JUMPER	28-7-65		



SCHEMATIC PHCO 4 FLIP FLOP



STRAY CAPACITANCE FROM THE COLLECTORS AND BASES TO THE EMITTERS OF THE TRANSISTORS SHOULD BE MINIMIZED.

UNIVAC

CIRCUIT, INTEGRATED, HYBRID (FLIP FLOP)

A P-HC-04

SHEET 2 OF 6

REVISIONS

ZONE	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D
—			7-8		

REQUIREMENTS:

GENERAL: HYBRID INTEGRATED CIRCUIT (FLIP FLOP)

PHYSICAL:

CONSTRUCTION: CONFORMAL EPOXY COATED OR EPOXY-FILLED PRE-MOLDED PLASTIC CASE

MARKINGS: UNIVAC PART NO., LEAD IDENTITY, EIA DATE CODE AND VENDOR IDENTIFICATION ON TOP OF UNIT

TERMINALS: TINNED COPPER

TERMINAL STRENGTH: PER MIL-STD-202C, METHOD 211, CODITION A (3 LBS.) AND CONDITION D

ELECTRICAL (AT 25°C ±2°C AMBIENT):

TRANSISTORS: PER 258-N1

DIODES: D1, D2: PER 258-D2

OTHERS: PER 258-D1

RESISTORS:

D.C. RESISTANCE: SEE SCHEMATIC

RESISTANCE TOLERANCE: ±1%

TEMPERATURE COEFFICIENT (BETWEEN -20°C AND +80°C): ±350 PPM/°C MAX.

POWER RATING AT 80°C, AS ENCAPSULATED: 25 MW MIN. PER RESISTOR

CAPACITORS:

CAPACITANCE AT IMC: SEE SCHEMATIC

CAPACITANCE TOLERANCE: ±10%

D.C. VOLTAGE: 25V MIN.

DISSIPATION FACTOR AT IMC: 1% MAX.

TEMPERATURE COEFFICIENT (BETWEEN -20°C AND +80°C): 500 PPM/°C MAX.

MODULE: INSULATION RESISTANCE, ANY PIN TO CASE AT 100 VDC: 50K MEG OHMS

ENVIRONMENTAL:

OPERATING TEMPERATURE RANGE: -20°C TO +80°C

STORAGE TEMPERATURE RANGE: (48 HOURS) +150°C

RELATIVE HUMIDITY: 100% RH, INCLUDING FROST OR WATER CONDENSATION

TEMPERATURE CYCLING: MUST MEET REQUIREMENTS OF MIL-STD-202, METHOD 107A, CONDITION A (EXCEPTION: ≥ 1 MINUTE BETWEEN TEMPERATURE EXTREMES). TEST PER TEST SPECIFICATION.

UNIVAC

DIVISION OF SPERRY RAND CORPORATION

PURCHASED PART DRAWING

CLASS A

TYPE SPECIFICATION CONTROL

TITLE CIRCUIT, INTEGRATED, HYBRID (FLIP FLOP)

CODE IDENT NO. 94209 CATALOG CODE

SIZE A

DWG NO. P-HC-04

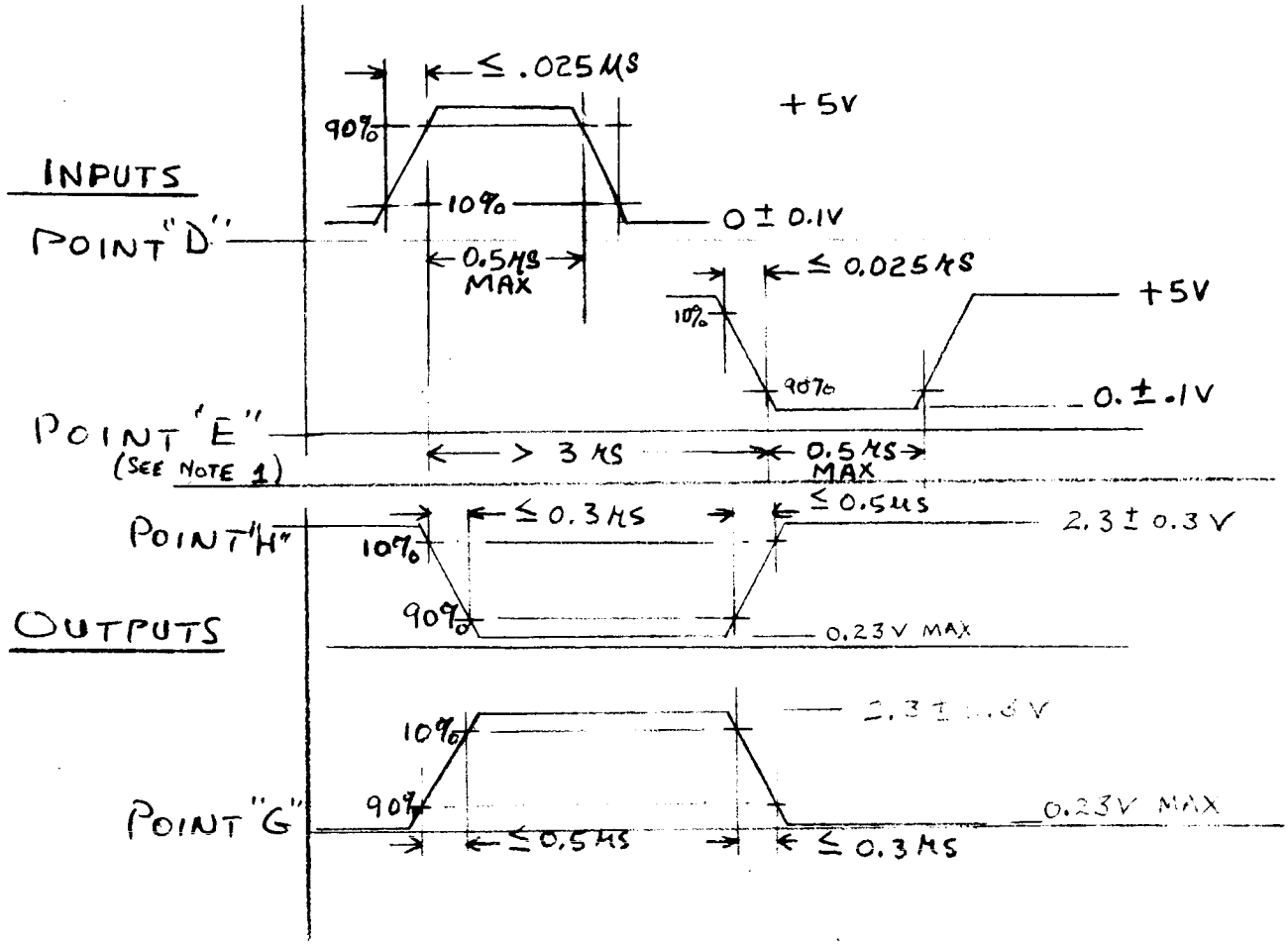
SHEET 3 OF 6

DWG. NO. P-HC-04

Electrical Tests:
Test #1:
Point A +5 Volts
Point B Ground

(All Switching Speeds measured with probe input impedance of 10 meg. shunted by a maximum of 9 uuf.
ALL Test Points Open Unless Specified)
All Voltage levels ± .1 OR ± 3%, Which-ever Is Larger.
Point C & L Must Be Connected For All Tests.

REVISIONS					
SYM	EIR	DESCRIPTION	DATE	CHK	APPD
–			7-8-65		
A		ADD. C & L INFO.	23-7-65		



Flip-Flop should set and reset with the maximum pulse width specified as inputs at points D and E.

Note 1: A diode should be placed in series with input E for all tests. Connect anode to Point E.

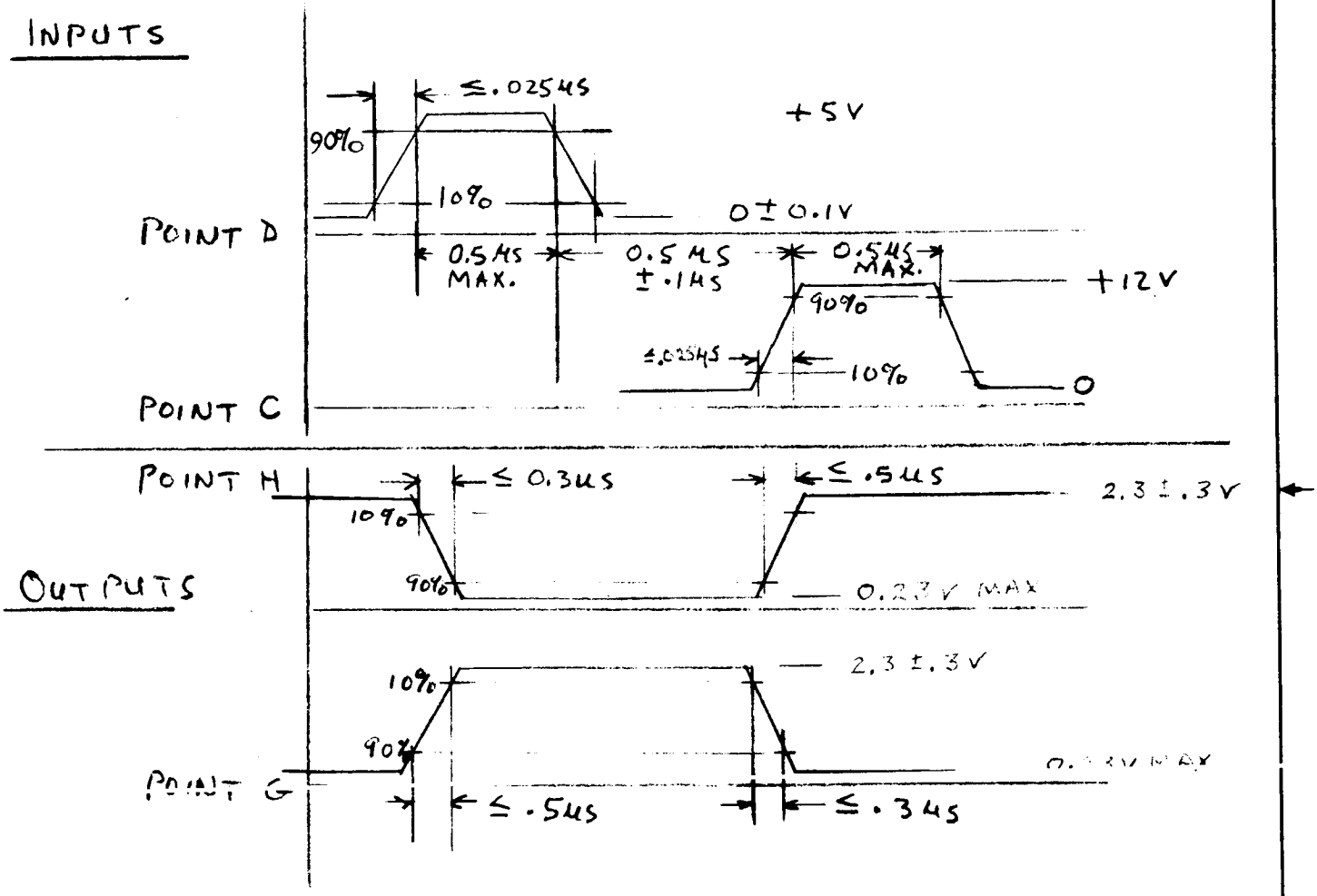
COMPONENT ENGINEER	DATE	CLASS	UNIVAC
DESIGN ENGINEER			PURCHASED PART DRAWING
QUALITY		TYPE	
STANDARDS		TITLE	CIRCUIT, INTEGRATED, HYBRID (FLIP FLOP)
		CODE IDENT NO.	SIZE A / DWG NO. P-HC-04
	WEIGHT	CATALOG CODE	SHEET 4 OF 6

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS IN INCHES
TOLERANCE ON FRACTIONS ± | DECIMALS ± | ANGLES ±

DWG. NO. P-HC-04

Test #2:
Point A +5 Volts
Point B Ground

REVISIONS					
SYM	EIR	DESCRIPTION	DATE	CHK	APPD
–			7-8		



COMPONENT ENGINEER	DATE	CLASS	UNIVAC
DESIGN ENGINEER			PURCHASED PART DRAWING
QUALITY		TYPE	
STANDARDS		TITLE	CIRCUIT, INTEGRATED, HYBRID (FLIP FLOP)
		CODE IDENT NO.	SIZE A / DWG NO. P-HC-04
	WEIGHT	CATALOG CODE	SHEET 5 OF 6

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS IN INCHES
TOLERANCE ON FRACTIONS ± | DECIMALS ± | ANGLES ±

REVISIONS					
SYM	E.I.R.	DESCRIPTION	DATE	CHK	APPD
A		DELETED TEST 6 AND 7	7-8 65		

TEST #3:

POINT A +5

POINT B GROUND

POINT C +12

POINT K 10K OHMS TO GROUND

POINT D +12

POINT I GROUND

OUTPUT AT POINT K < .6 VOLTS

THE PULSING OF INPUT F FROM 0 TO +12 VOLTS FOR 1.0 ±0.1μSEC SHOULD NOT EFFECT OUTPUT K.

TEST #4:

POINT A +5

POINT B GROUND

POINT C +12

POINT K 10KΩ TO GROUND

OUTPUT AT POINT K > 2.5 VOLTS

THE PULSING OF INPUT F FROM 0 TO +12 VOLTS FOR 1.0 ±0.1μSEC SHOULD NOT EFFECT OUTPUT K.

TEST #5:

CONNECT 10KΩ RESISTORS BETWEEN +12V AND POINTS G AND H. GROUND POINT B. THE TOTAL CURRENT FROM THE +12-VOLT SUPPLY SHALL NOT EXCEED 0.1μ AMP.

COMPONENT ENGINEER	DATE	CLASS	UNIVAC
DESIGN ENGINEER			PURCHASED PART DRAWING
QUALITY		TYPE	
STANDARDS		TITLE	CIRCUIT, INTEGRATED, HYBRID (FLIP FLOP)
		CODE IDENT NO.	SIZE A — DWG NO. P-HC-04
	WEIGHT	CATALOG CODE	SHEET 6 OF 6

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS IN INCHES
TOLERANCE ON FRACTIONS ± | DECIMALS ± | ANGLES ±

P-HC-05

COUNTER STAGE

PROJECT 258

UNIVAC

PURCHASE SPECIFICATION FOR CIRCUIT, INTEGRATED, HYBRID

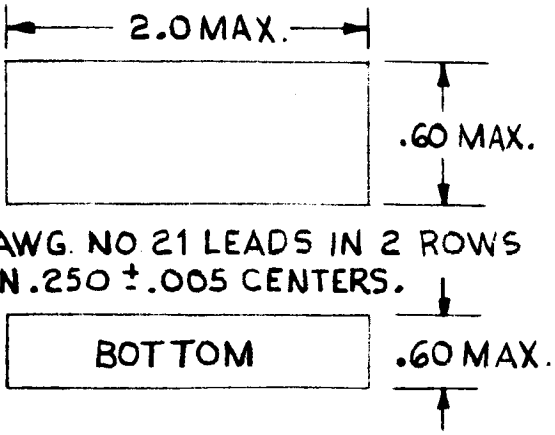
A P-HC-05

SHEET 1 OF 7

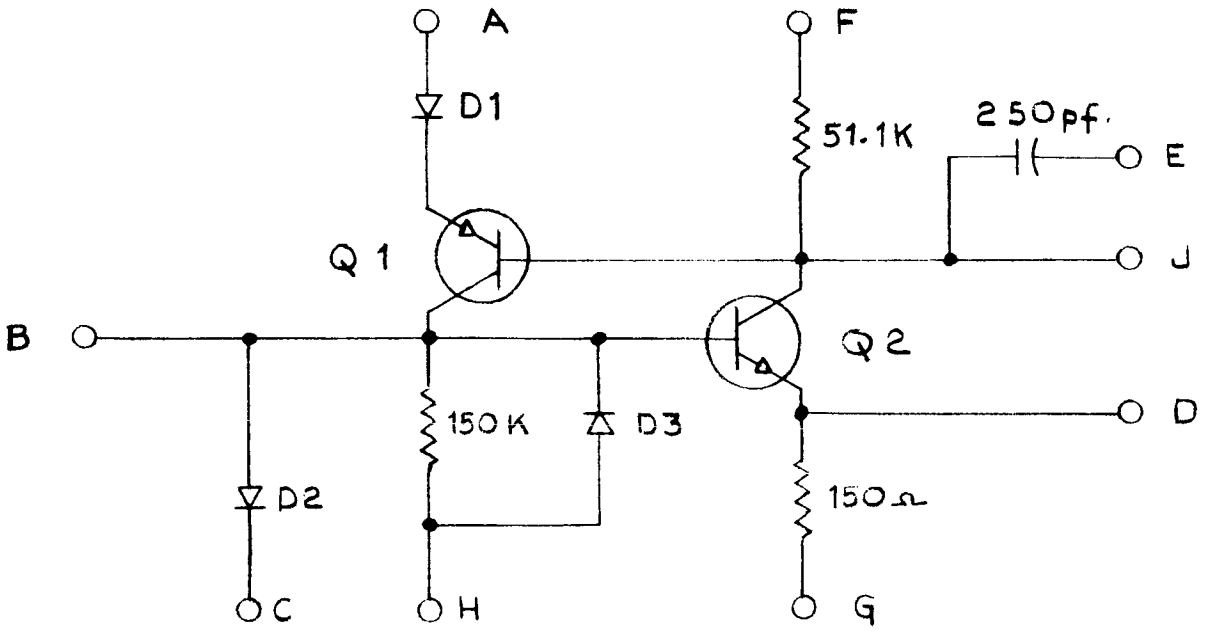
P-HC-05

ELECTRICAL, MECHANICAL OPTION A

MECHANICAL OUTLINE



ELECTRICAL SCHEMATIC



SINGLE STAGE

UNIVAC

CIRCUIT, INTEGRATED, HYBRID

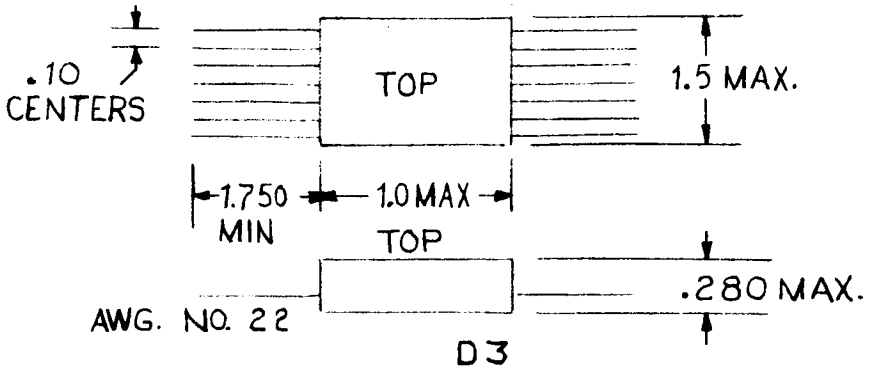
P-HC-05

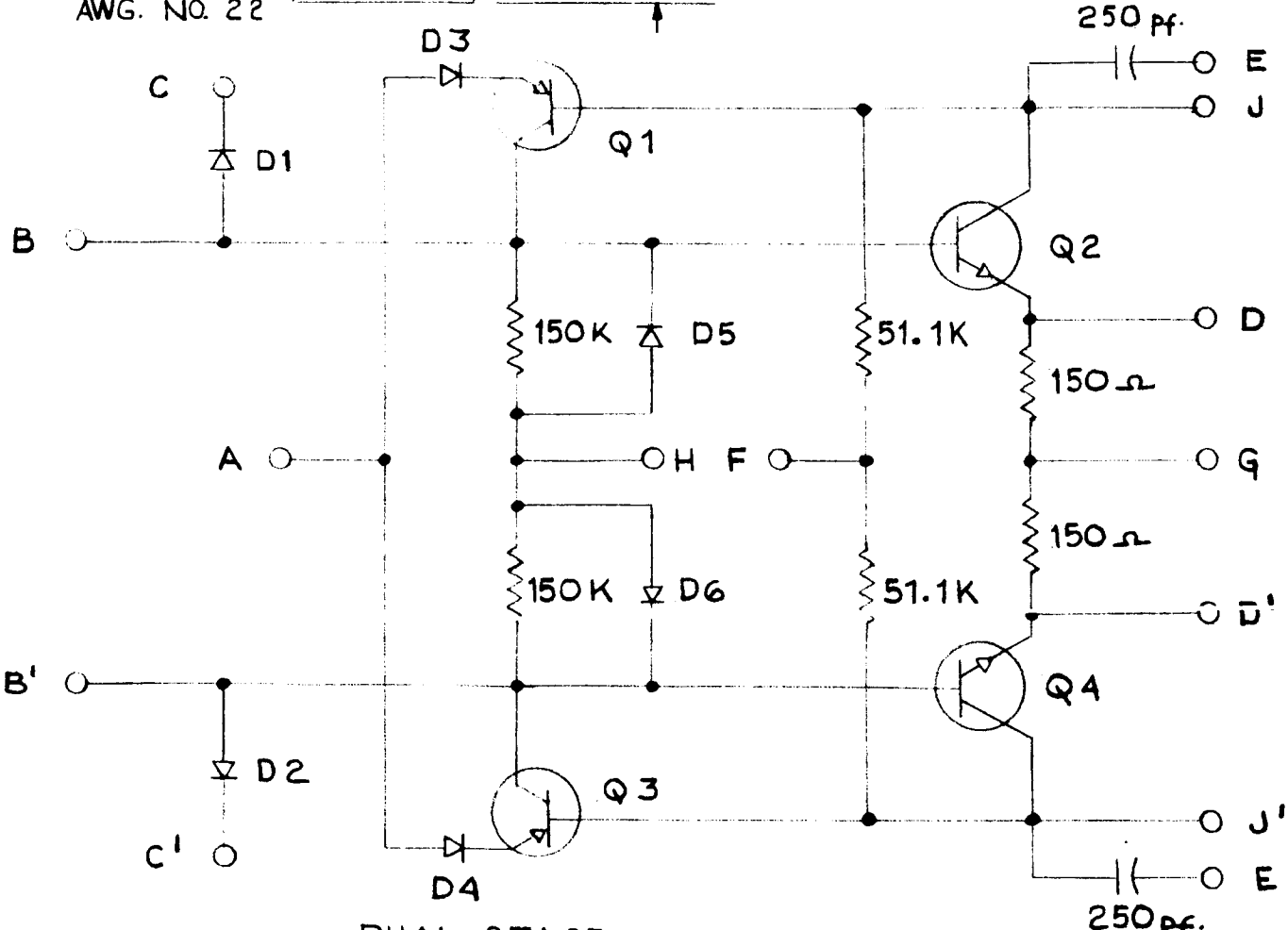
SHEET 2 OF 7

P-HC-05

ELECTRICAL, MECHANICAL OPTION B

MECHANICAL OUTLINE





DUAL STAGE
ELECTRICAL SCHEMATIC

UNIVAC

CIRCUIT, INTEGRATED, HYBRID

A P-HC-05

SHEET 3 OF 7

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	DES	APVD

REQUIREMENTS: (OPTION A OR B)

GENERAL: HYBRID INTEGRATED CIRCUIT (COUNTER STAGE)

PHYSICAL:

CONSTRUCTION: CONFORMAL EPOXY COATED, OR EPOXY-FILLED PRE-MOLDED PLASTIC CASE

MARKINGS: UNIVAC PART NO., LEAD IDENTITY, EIA DATE CODE, AND VENDOR IDENTIFICATION ON TOP OF UNIT.

TERMINALS: TINNED COPPER

TERMINAL STRENGTH: MUST MEET MIL STD-202C, METHOD 211, CONDITION A (3 LBS.) AND CONDITION D

ELECTRICAL: (AT 25 $\pm 2^{\circ}$C AMBIENT)

TRANSISTORS: Q1, Q3 - PER 258 - P1; Q2, Q4 - PER 258 - N1

DIODES: PER 258 - D1

RESISTORS: (SEE SCHEMATIC FOR D.C. VALUES)

TOLERANCE: $\pm 3\%$

TEMPERATURE COEFFICIENT: (BETWEEN -20°C AND $+80^{\circ}$C): ± 350PPM/$^{\circ}$C MAX.

POWER RATING AT 80°C, AS ENCAPSULATED: 25MW PER RESISTOR

CAPACITORS: (SEE SCHEMATIC FOR VALUE AT 1KC)

TOLERANCE: $\pm 5\%$

D.C. VOLTAGE RATING: 25V MINIMUM

LEAKAGE CURRENT AT 25VDC, 80°C: 0.1μA MAXIMUM

DISSIPATION FACTOR AT 1KC: 2.5% MAXIMUM

TEMPERATURE COEFFICIENT: (BETWEEN -20°C AND $+80^{\circ}$C): -750PPM/$^{\circ}$C MAX.

MODULE: INSULATION RESISTANCE, ANY PIN TO CASE AT 100VDC: 50K MEGΩ

ENVIRONMENTAL:

OPERATING TEMPERATURE RANGE: -20°C TO $+80^{\circ}$C

STORAGE TEMPERATURE RANGE: (48 HOURS) $+150^{\circ}$C

RELATIVE HUMIDITY: 100% RH, INCLUDING FROST OR WATER CONDENSATION.

TEMPERATURE CYCLING: MUST MEET REQUIREMENTS OF MIL-STD-202, METHOD 107A, CONDITION A (EXCEPTION: $\leq$ 1 MINUTE BETWEEN TEMPERATURE EXTREMES). TEST PER TEST SPECIFICATION.

UNIVAC

CIRCUIT, INTEGRATED, HYBRID

SIZE A

P-HC-05

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	DES	APPD

ELECTRICAL TEST SPECIFICATIONS: (AT +25 $\pm 2^{0}$C)

A. OPTION A TYPE MODULES:

1. THE COUNTER STAGE SHALL BE TESTED IN GROUPS OF FOUR STAGES, (FOUR MODULES) INTERCONNECTED SO THAT TERMINAL E OF EACH STAGE IS CONNECTED TO TERMINAL B OF THE FOLLOWING STAGE. TERMINAL E OF THE FOURTH STAGE CONNECTS TO TERMINAL B OF THE FIRST STAGE. ON EACH STAGE, CONNECT A IN3207 DIODE BETWEEN TERMINAL D (ANODE) AND TERMINAL G (CATHODE). CONNECT THE TEST CIRCUIT TO THE STAGES UNDER TEST AS INDICATED IN FIGURE 1. CONNECT TERMINALS F TO +12 VOLTS D.C.; TERMINALS H TO -3 VOLTS D.C.; TERMINALS G TO GROUND. THE OUTPUT OF EACH STAGE IS VIEWED AT TERMINAL J.

2. ENERGIZE INPUT III AS INDICATED. AFTER 150 USEC. BEYOND THE FALL OF THE INPUT, THE OUTPUT OF STAGE ONE SHALL BE AT LESS THAN +0.6 VOLTS THE OUTPUTS OF ALL OTHERS STAGES SHALL BE AT +12 VOLTS.

3. ENERGIZE INPUT I ONCE AS INDICATED. THE OUTPUTS OF STAGES ONE, THREE AND FOUR SHOULD GO TO +12 VOLTS AND THE OUTPUT OF STAGE TWO SHALL BE 0.6 VOLT. UPON SUCCESSIVE APPLICATIONS OF INPUT I THE STAGE WITH A LOW OUTPUT SHOULD PROGRESS TO STAGES 3, 4, 1 ETC. ONLY ONE STAGE AT A TIME SHALL HAVE A LOW OUTPUT IN THE STEADY STATE CONDITION. THIS SHALL BE TESTED AT STEP RATES OF 70 USEC. AND 1MSEC.

4. ENERGIZE INPUT II WHILE VIEWING THE STAGE WITH LOW OUTPUT. THIS SHOULD BE DONE NOT LESS THAN 15 USEC. AFTER THE APPLICATION OF INPUT I. WHILE INPUT II IS ENERGIZED, A STEP IN THE OUTPUT OF THAT STAGE OF AT LEAST +0.5V MUST OCCUR. AFTER INPUT II FALLS, THE SYSTEM SHALL NOT HAVE CHANGED STATE. REPEAT THIS TEST FOUR TIMES TO CHECK EACH OF THE FOUR STAGES.

B. OPTION B TYPE MODULES:

1. SAME AS 1 ABOVE EXCEPT AS FOLLOWS (TWO MODULES, 4 STAGES): CONNECT TERMINALS E TO TERMINALS B' OF SAME MODULE, E' OF FIRST MODULE TO B OF SECOND, E' OF SECOND TO B OF FIRST. ADD IN3207 DIODES BETWEEN D' (ANODE) AND G, AND D (ANODE) AND G OF EACH MODULE. OUTPUT IS VIEWED AT J AND J'.

2-4 SAME AS ABOVE.

UNIVAC

CIRCUIT, INTEGRATED HYBRID

A P-HC-05

SHEET 5 OF 7

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	DES	APPD

ELECTRICAL TEST SPECIFICATIONS: (CONT.)

C. OPTION A AND B TYPE MODULES

PERFORM THE FOLLOWING TEST ON EACH MODULE INDIVIDUALLY; CONNECT TERMINAL G TO GROUND, TERMINAL F TO +12V, TERMINAL H TO -3V AND TERMINAL A THROUGH 5KΩ TO +2V. IN APPLYING THE VOLTAGES, TURN ON THE +2V LAST, AND BRING IT UP SLOWLY. IF THE CURRENT DRAWN FROM THE +2V SUPPLY EXCEEDS 0.1 MA, THEN MOMENTARILY SHORT TERMINAL B (AND B' OF OPTION B MODULES) TO -3V. READ THE LEAKAGE CURRENT WHICH FLOWS THROUGH TERMINAL H. IT MUST NOT EXCEED 0.05 MICROAMPERES FOR OPTION A MODULES OR 0.10 MICROAMPERES FOR OPTION B MODULES.

ORIGINATOR DESIGN	DATE	CLASS	UNIVAC
PROJ. ENGINEER			PURCHASED PART DRAWING
QUALITY		TYPE	
STANDARDS		TITLE	CIRCUIT, INTEGRATED HYBRID
		CODE IDENT NO.	SIZE: A — DWG NO.: P-HC-05
	WEIGHT	CATALOG CODE	SHEET 6 OF 7

ALL DIMENSIONS IN INCHES
TOLERANCE ON FRACTIONS | DECIMALS | ANGLES

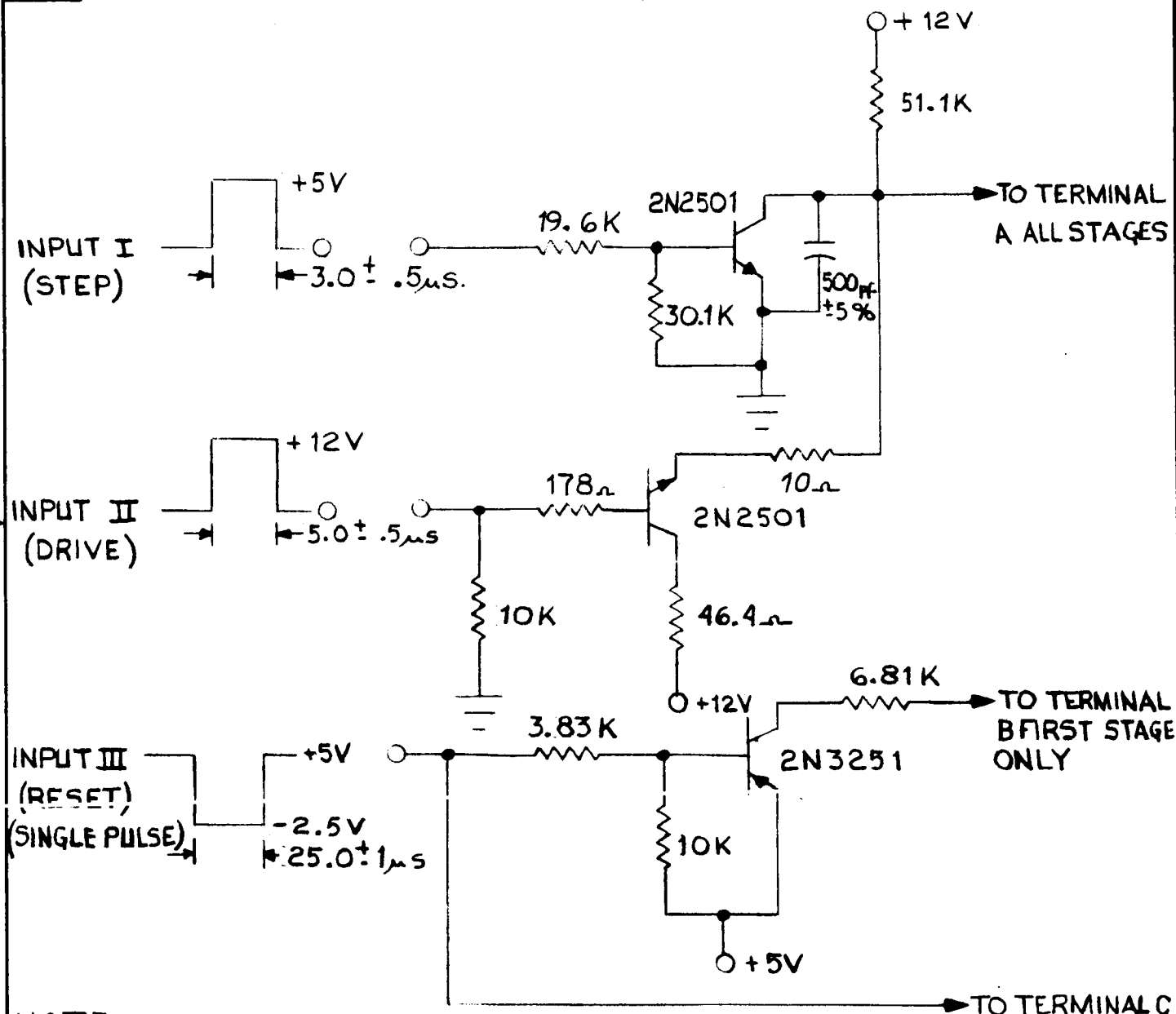
P-HC-05

TEST CIRCUIT

THE CIRCUITS OUTLINED BELOW SHALL BE USED FOR TESTING THE COUNTER STAGE.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	DES	APVD



NOTE: ALL RISE AND FALL TIMES ≤ 25 ns.
ALL RESISTORS, FILM, ± 1%.

FIG. 1. SCHEMATIC OF TEST CIRCUITS FOR COUNTER.

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CIRCUIT, INTEGRATED HYBRID

A P-HC-05

SHEET 7 OF 7

P-HC-06

REVISIONS					
ZONE	ECR	DESCRIPTION	DATE	BY	APVD
—			4-25		

P-HC-06

PULSE AMPLIFIER

PROJECT 258

R. Grossman	4/16/65	CLASS —	UNIVAC
C. A. Nelson	4/16/65		PURCHASED PART DRAWING
		TYPE	
		TITLE	CIRCUIT, INTEGRATED, HYBRID (PULSE AMPLIFIER)
		CODE IDENT NO.	SIZE A — DWG NO. P-HC-06
		CAVLOS CODE	SHEET 1 OF 6

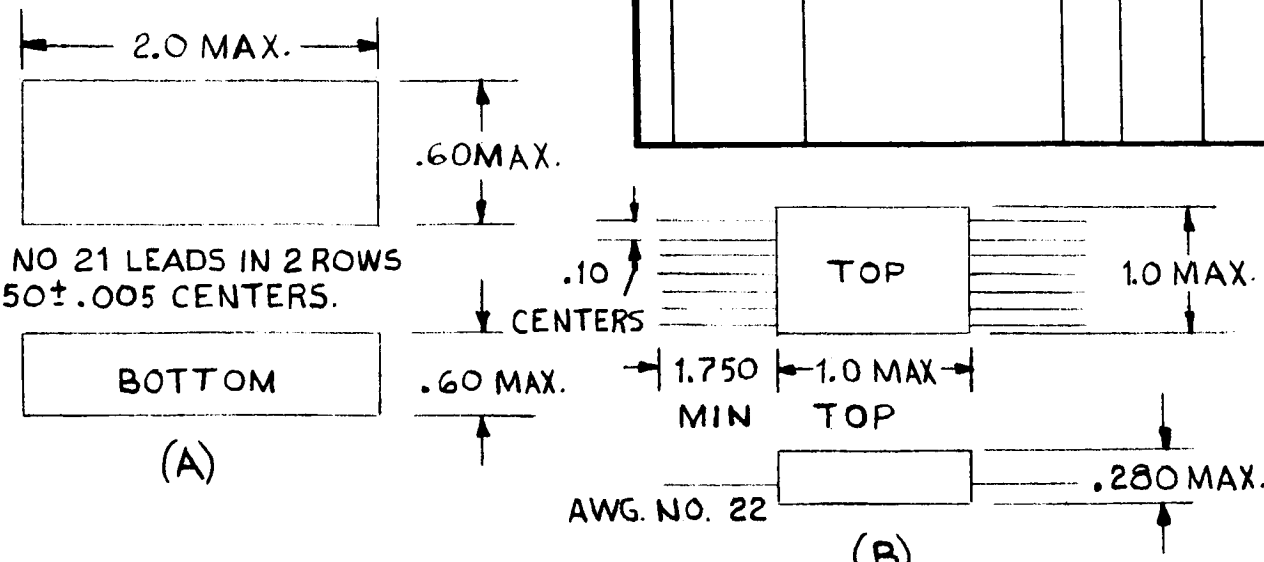
UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS IN INCHES
TOLERANCE ON
FRACTIONS | DECIMALS | ANGLES

P-HC-06

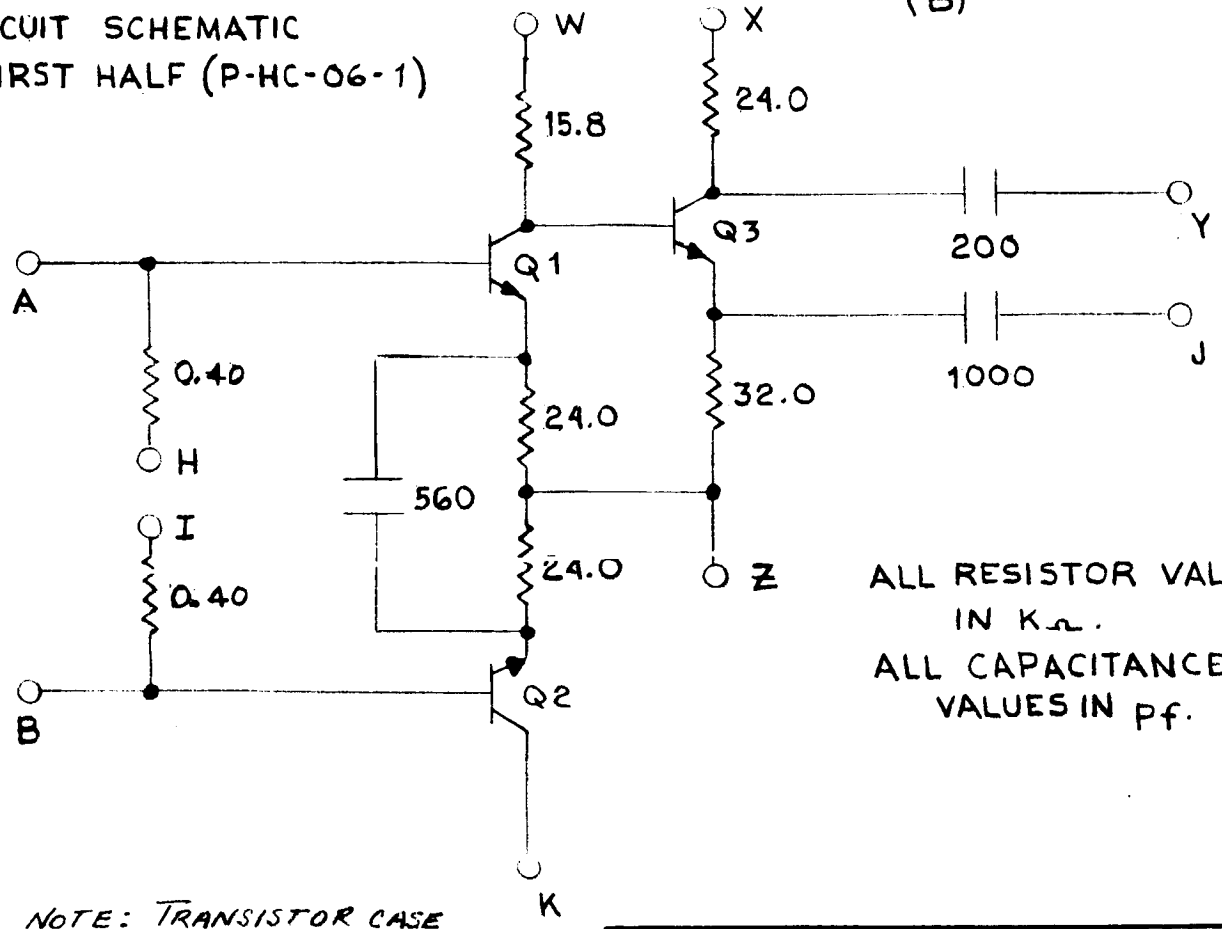
REVISIONS

SYM	ECR	DESCRIPTION	DATE	CHK	APPD

MECHANICAL OUTLINE (A OR B)



CIRCUIT SCHEMATIC FIRST HALF (P-HC-06-1)



ALL RESISTOR VALUES IN KΩ.
ALL CAPACITANCE VALUES IN pf.

NOTE: TRANSISTOR CASE LEAD SHALL BE CONNECTED TO NEAREST GROUND PIN H, I OR J

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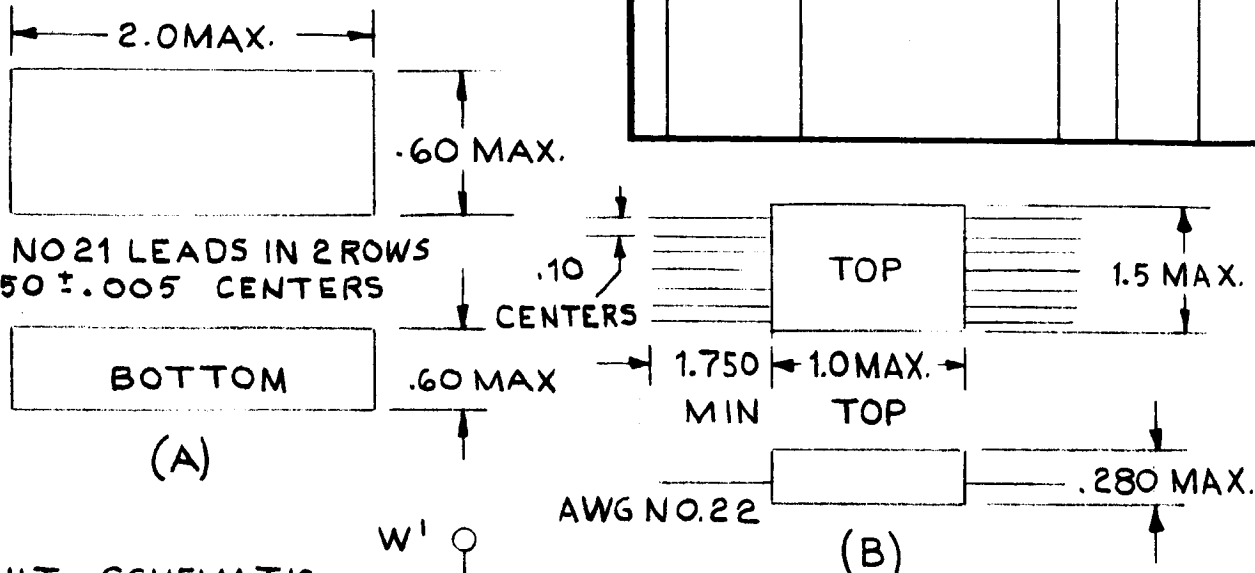
CIRCUIT, INTEGRATED, HYBRID (PULSE AMPLIFIER)

A P-HC-06

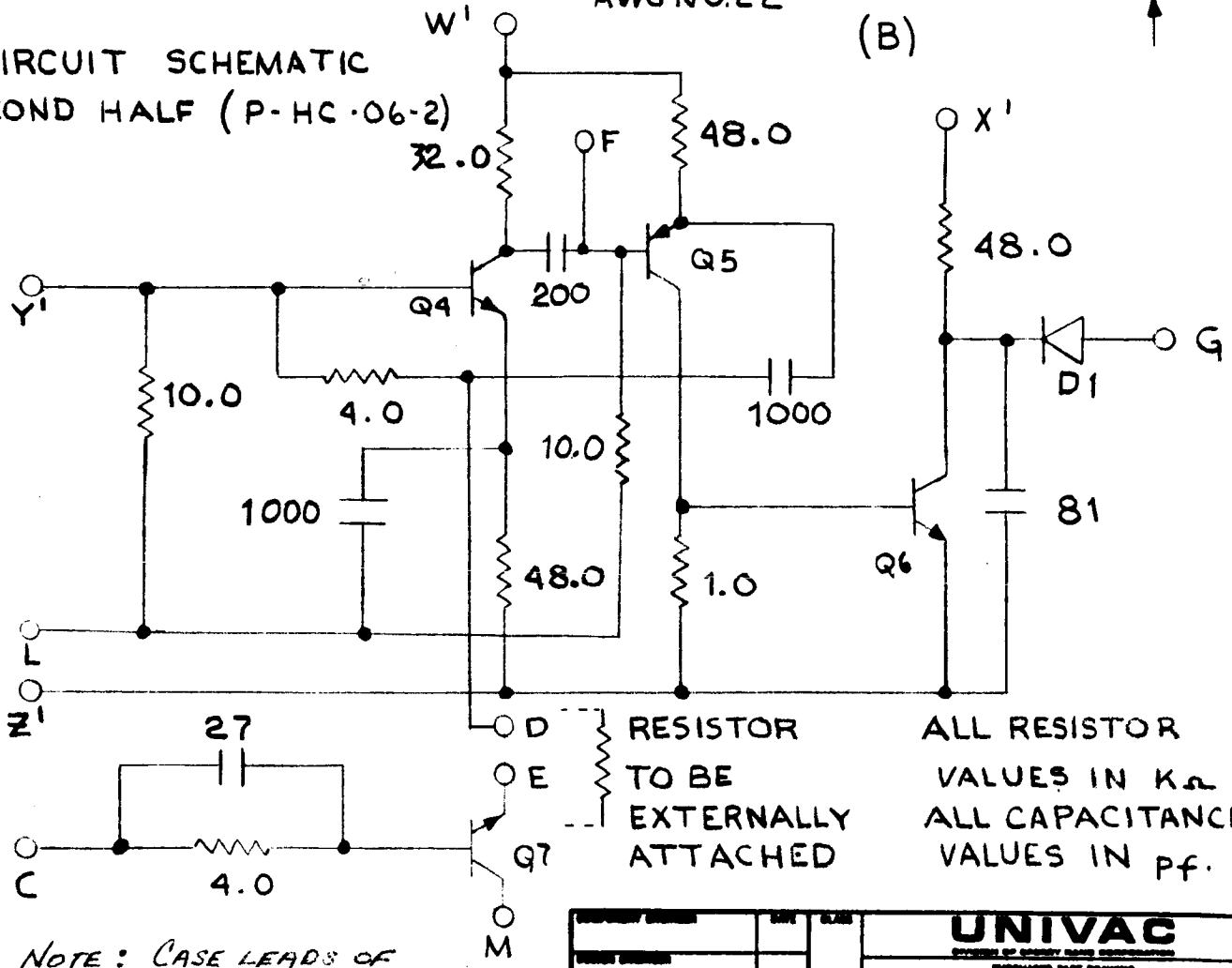
SHEET 2 OF 6

P-HC-06

MECHANICAL OUTLINE
(A OR B)



CIRCUIT SCHEMATIC
SECOND HALF (P-HC-06-2)



RESISTOR TO BE EXTERNALLY ATTACHED

ALL RESISTOR VALUES IN KΩ
ALL CAPACITANCE VALUES IN pf.

NOTE: CASE LEADS OF Q4 AND Q7 SHALL BE CONNECTED TO NEAREST GROUND PIN L OR M

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DIVISION OF SPERRY RAND CORPORATION
PURCHASED PART DRAWING

CIRCUIT, INTEGRATED, HYBRID (PULSE AMPLIFIER)

A P-HC-06

SHEET 3 OF 6

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	DES	APPD

REQUIREMENTS:

GENERAL: HYBRID INTEGRATED CIRCUIT (PULSE AMPLIFIER)

PHYSICAL:

CONSTRUCTION: CONFORMAL EPOXY COATED, OR EPOXY-FILLED PRE-MOLDED PLASTIC CASE

MARKINGS: UNIVAC PART NO. LEAD IDENTITY, EIA DATE CODE AND VENDOR IDENTIFICATION ON TOP OF UNIT

TERMINALS: TINNED COPPER

TERMINAL STRENGTH: MUST MEET MIL-STD-202C, METHOD 211, CONDITION A (3 LBS.) AND CONDITION D

ELECTRICAL (AT 25 $\mp 2^{\circ}$C AMBIENT):

TRANSISTORS: Q1-Q4, Q7-PER 258-N2, Q5-PER 258-P1; Q6-PER 258-N1

DIODE: PER 258-D1

RESISTORS: (SEE SCHEMATIC FOR D.C. VALUES)

TOLERANCE: $\pm 1\%$

TEMPERATURE COEFFICIENT (BETWEEN -20°C AND $+80^{\circ}$C): ± 350 PPM/$^{\circ}$C MAX.

DISSIPATION RATING AT 80°C AS ENCAPSULATED: 25 MW MIN. PER RESISTOR

CAPACITORS (SEE SCHEMATIC FOR CAPACITANCE VALUES):

$\leq$81PF AT 1MC; $\geq$200PF AT 1KC

TOLERANCE: $\pm 10\%$

D.C. VOLTAGE RATING: 25V MIN.

TEMPERATURE COEFFICIENT (BETWEEN -20°C AND $+80^{\circ}$C):

$\leq$81PF: $\pm$300PPM/ C MAX; $\geq$200PF: $\pm 5\%$ MAX.

DISSIPATION FACTOR: $\leq$ 81PF: 1.0% MAX., $\geq$ 200PF: 2.5% MAX.

MODULE: INSULATION RESISTANCE, ANY PIN TO CASE AT 100 VDC: 50K MEG OHMS

ENVIRONMENTAL:

OPERATING TEMPERATURE RANGE: -20°C TO $+80^{\circ}$C

STORAGE TEMPERATURE RANGE (48 HOURS): $+150^{\circ}$C

RELATIVE HUMIDITY: 100% RH, INCLUDING FROST OR WATER CONDENSATION

TEMPERATURE CYCLING: MUST MEET REQUIREMENTS OF MIL-STD-202, METHOD 107A, CONDITION A (EXCEPTION: $\leq$ 1 MINUTE BETWEEN TEMPERATURE EXTREMES). TEST PER TEST SPECIFICATION.

UNIVAC

CIRCUIT, INTEGRATED, HYBRID (PULSE AMPLIFIER)

A P-HC-06

SHEET 4 OF 6

ELECTRICAL TESTS (25 ±2°C AMBIENT):

A. CONNECT MODULE HALVES: X TO X', Y TO Y', Z TO Z'. GROUND H, I, J, L AND M. APPLY +3.0V TO WW' AND K, -3V TO ZZ', AND 6V TO XX'.

CONNECT A 100 OHM RESISTOR BETWEEN TERMINALS D AND E. CONNECT THE OUTPUT TEST CIRCUIT. THE FOLLOWING TESTS ARE TO BE CONDUCTED AT ROOM TEMPERATURE:

I. APPLY +6 VOLTS TO TERMINAL C. CONNECT THE INPUT TEST CIRCUIT TO THE CIRCUIT UNDER TEST.

A) APPLY A POSITIVE 1.4V INPUT TO TERMINAL I OF THE INPUT TEST CIRCUIT. THE APPLICATION OF THE INPUT SHALL CAUSE AN OUTPUT AT TERMINAL G AS SHOWN IN THE WAVESHAPES FOR TEST I.

B) REPEAT (A) APPLYING A NEGATIVE 1.4V INPUT TO TERMINAL (2) OF THE INPUT TEST CIRCUIT.

C) APPLY A POSITIVE 7.0 VOLT INPUT TO TERMINALS (1) AND (2) OF THE INPUT TEST CIRCUIT. THE APPLICATION OF THIS INPUT SHALL CAUSE NO OUTPUT AT TERMINAL G.

II. GROUND TERMINAL C. APPLY A 2 VOLT POSITIVE PULSE TO TERMINAL A. THE WIDTH OF THE INPUT PULSE IS 100 NS., ±10 NS, AND THE RISE AND FALL TIME ARE LESS THAN 10 NS. THE APPLICATION OF THE INPUT PULSE SHALL CAUSE NO OUTPUT AT TERMINAL G.

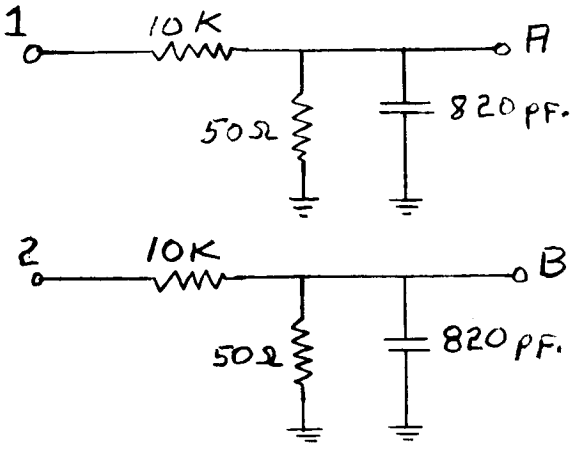
B. I. FIRST HALF: P-HC-06-1

GROUND TERMINALS H AND I. APPLY -3V TO Z, +3V TO W AND K, AND +6V TO X. THE CURRENT FLOWING (A) FROM Z SHALL NOT EXCEED 350μA, (B) INTO W AND K SHALL NOT EXCEED 230μA, AND (C) INTO X SHALL NOT EXCEED 130μA.

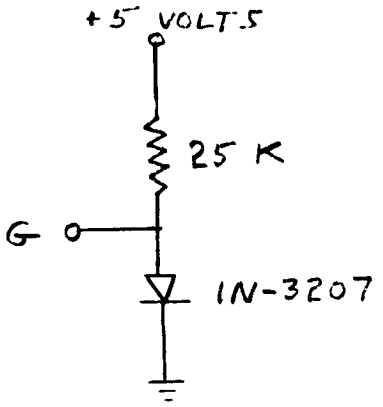
II. SECOND HALF: P-HC-06-2
GROUND TERMINAL L. APPLY -3V TO Z', +3V TO W' AND +6V TO X'. THE CURRENT FLOWING (A) FROM Z' SHALL NOT EXCEED 120μA, (B) INTO W' SHALL NOT EXCEED 120μA, AND (C) INTO X' SHALL NOT EXCEED 1μA.

DWG. NO. P-HC-06

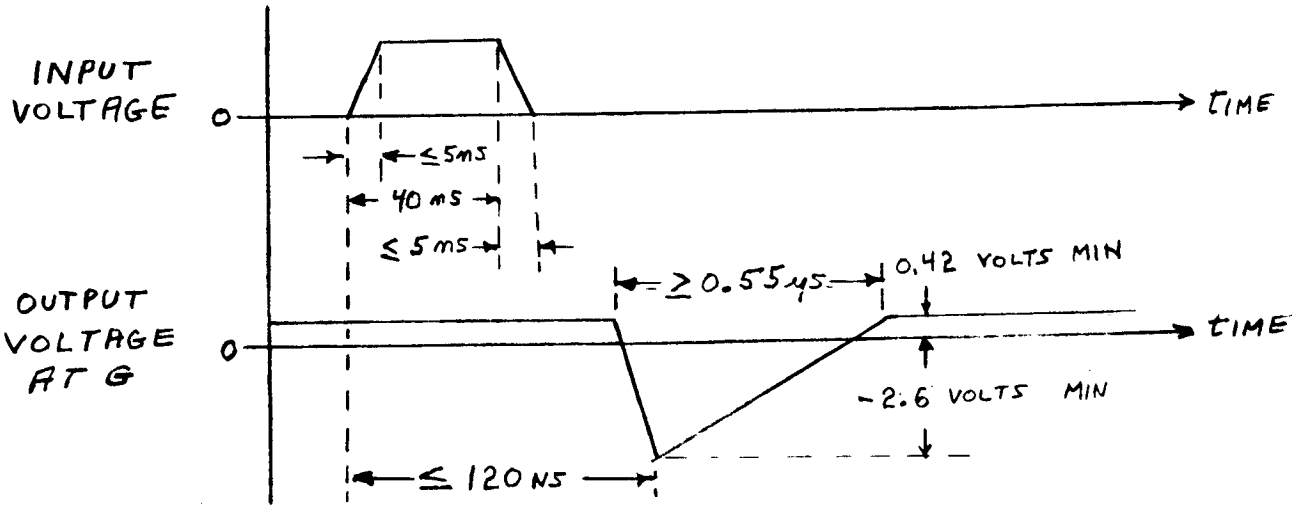
REVISIONS					
SYM	E.I.R.	DESCRIPTION	DATE	CHK	APPD



INPUT TEST CIRCUIT



OUTPUT TEST CIRCUIT



WAVESHAPES FOR TEST I

COMPONENT ENGINEER	DATE	CLASS	UNIVAC
DESIGN ENGINEER			PURCHASED PART DRAWING
QUALITY		TYPE	
STANDARDS		TITLE	CIRCUIT, INTEGRATED, HYBRID (PULSE AMPLIFIER)
		CODE IDENT NO.	SIZE: A — DWG NO.: P-HC-06
	WEIGHT	CATALOG CODE	SHEET 6 OF 6

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS IN INCHES
TOLERANCE ON FRACTIONS * DECIMALS * ANGLES *

258-N3

Transistors for testing to this procedure shall be Fairchild Type 2N3302.

Outline: TO-18

CHARACTERISTIC (conditions)	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
1. Collector-Emitter Sustaining Voltage (I_C = 10 mA, pulsed, I_B = 0)	V_{CEO} (Sust.)	30		Vdc
2. Emitter-Base Breakdown Voltage (I_C = 0, I_E = 10 uAdc)	BV_{EBO}	5.0		Vdc
3. Collector-Emitter Saturation Voltage (I_C = 500 ma., I_B = 50 ma.)	V_{CE} (Sat.)		.53	Vdc
4. Base-Emitter Saturation Voltage (I_C = 500 ma., I_B = 50 ma.)	V_{BE} (Sat.)		1.35	Vdc
5. DC Pulsed Current Gain (I_C = 500 mA., pulsed, V_{CE} = 5V)	h_{FE}	50		

258-P2

Transistors for testing to this procedure shall be Fairchild Type 2N3504.

Outline: TO-18

CHARACTERISTIC (conditions)	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT
1. Collector-Emitter Sustaining Voltage (I_C = 10 mA., pulsed, I_B = 0)	V_{CEO} (Sust)	-45		Vdc
2. Emitter-To-Base Breakdown Voltage (I_E = 10 uAdc, I = 0)	BV_{EBO}	-5.0		Vdc
3. Collector-Emitter Saturation Voltage (I_C = 60 mAdc, I_B = 2.0 mAdc)	V_{CE} (Sat.)		-0.20	Vdc
4. Base-Emitter Saturation Voltage (I_C = 60 mAdc, I_B = 2.0 mAdc)	V_{BE} (Sat).		-0.95	Vdc

Diode 258-D1

Diodes purchased for testing to this procedure shall be MicroSemiconductor Type 1N3207.

ELECTRICAL TESTS:

	CHARACTERISTIC (Conditions)	SYMBOL	LIMIT MIN.	LIMIT MAX.	UNITS
1	Reverse Current (V_R = 20V dc)	I_R		.05	uAdc
2	Forward Voltage (I_F = 200 uAdc)	V_F	.45	.55	Vdc
	(I_F = 5 uAdc)		.30	.40	Vdc
	(I_F = 10 mAdc)		.65	.75	Vdc

A MI 4/13/..

Diode 258-D2

Diodes purchased for testing to this procedure shall be General Electric Type 1N4156.

ELECTRICAL TESTS:

	CHARACTERISTIC (Conditions)	SYMBOL	LIMIT MIN.	LIMIT MAX.	UNITS
1	Forward Voltage (I_F = 10 ua)	V_F	0.74		Vdc
	(I_F = 100 ua)			1.22	Vdc

Transistor 258-N1

Transistors purchased for testing to this procedure shall be Motorola Type 2N2501.
Case: TO-18

ELECTRICAL TESTS:

CHARACTERISTIC (Conditions)	SYMBOL	LIMIT MIN.	LIMIT MAX.	UNITS
1. Collector-Emitter Breakdown Voltage (I_C = 30 ma., I_B = 0, Pulsed)	BV_{CEO}	20		Vdc
2. Collector Leakage Current (V_{CE} = 12V, R_{BE} = 100 K Ohms)	I_{CEX}		30	nAdc
3. Emitter-Base Breakdown Voltage (I_E = 10 uAdc, I_C = 0)	BV_{EBO}	7		Vdc
4. Emitter Leakage Current (V_{EB} = 6 Vdc)	I_{EBO}		30	nAdc
5. DC Forward Current Transfer Ratio (I_C = 0.6 mA, V_{CE} = 0.3V) (I_C = 50 mA, V_{CE} = 0.35V)	h_{FE}	30 30		
6. Collector-Emitter Saturation Voltage (I_C = 0.2 mA, I_B = 0.02 mA)	V_{CE} (Sat)		0.28	Vdc
7. Base-Emitter Saturation Voltage (I_C = 0.2 mA, I_B = 0.02 mA)	V_{BE} (Sat)		0.7	Vdc
8. Charge Storage Time Constant ($I_C = I_{B1} = I_{B2}$ = 10 mAdc, refer to Motorola data sheet, 2N2501 for test circuit schematic).	τ_S		15	nsec.

Transistor 258-N2

Transistors for testing to this procedure shall be Motorola Type 2N3493.
Case: TO-18 (4 Leads)

	CHARACTERISTIC (Conditions)	SYMBOL	MIN.	MAX.	UNIT
1.	Collector-Base Breakdown Voltage (I_C = 10 ua, I_E = 0)	BV_{CBO}	12		Vdc
2.	DC Forward Current Gain (I_C = 100 uA, V_{CE} = 0.5V)	h_{FE}	40		
3.	Base-Emitter Saturation Voltage (I_C = 100 uA, I_B = 10 uA)	V_{BE} (Sat)		0.75	Vdc
4.	High Frequency Current Gain (I_C = 1 mA, V_{CE} = 3V, f = 100 mc)	h_{fe}	4.0		
5.	Output Capacitance (V_{CB} = 3V, I_E = 0, f = 100kc)	C_{ob}		0.7	pf
6.	Input Capacitance (V_{EB} = 0.5V, I_C = 0, f = 100kc)	C_{ib}		0.7	pf
7.	Saturated Dynamic Impedance (I_B = 1 mA, I_E = 100 uA peak, f = 100kc)	R_{ec}		50	ohms

4/10/63 R III

Transistor 258-P1

Transistors purchased for testing to this procedure shall be Motorola 2N3251.
Case: To-18

ELECTRICAL TESTS:

	CHARACTERISTIC (Conditions)	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
1.	Collector-Base Breakdown Voltage (I_C = 10 ua.)	BV_{CBO}	50		Vdc
2.	Collector Leakage Current (V_{CE} = 40V, V_{BE} = -3V)	I_{CEX}		20	nAdc
3.	Base Leakage Current (V_{CE} = 40V, V_{BE} = -3V)	I_{BL}		50	nAdc
4.	Emitter-Base Breakdown Voltage I_E = 10 ua)	BV_{EBO}	5.6		Vdc
5.	Collector Saturation Voltage (I_C = 50 ma., I_B = 5 ma.)	V_{CE} (Sat)		.5	Vdc
6.	Base-Emitter Saturation Voltage (I_C = 10 ma., I_B = 1 ma.)	V_{BE} (Sat)	0.6	0.9	Vdc
7.	DC Forward Current Transfer Ratio (I_C = 0.1 ma., V_{CE} = 1V)	h_{FE}	80		
8.	Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 KC)	C_{ob}		6	pf
9.	Input Capacitance (V_{EB} = 1 Vdc, I_C = 0, f = 100 KC)	C_{ib}		8	pf
10.	Current Gain-Bandwidth Product (V_{CE} = 20Vdc, I_C = 10 mAdc, f = 100 mc)	f_t	300		mc

Transistor 258-C1

Source: Motorola NPN Chip Type SL-1

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	MAX.	UNITS
I_{EBO}	Emitter Leakage Current	$I_C = 0$, $V_{EB} = 3V$		20	nA.
I_{CBO}	Collector Leakage Current	$I_E = 0$, $V_{CB} = 3V$		10	nA.
H_{FE}	DC Current Gain	$I_C = 30ma$, $V_{CE} = 0.5V$	35		
V_{BE} (Sat)	Base Saturation Voltage	$I_C = 0$, $I_B = 1.5$ ma.		.90	Volts
C_{ie}	Emitter Capacitance	$I_C = 0$, $V_{EB} = 3V$, f = 1mc		5	pf.

Transistor 258-C2

Source: Motorola PNP Chip Type SL-44

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	MAX.	UNITS
I_{EBO}	Emitter Leakage Current	$I_C = 0$, $V_{EB} = 3V$		20	NA
I_{CBO}	Collector Leakage Current	$I_E = 0$, $V_{CB} = 3V$		10	NA
H_{FE}	DC Current Gain	$I_C = 30$ ma, $V_{CE} = 0.5V$	35		
V_{BE} (Sat)	Base Saturation Voltage	$I_C = 0$, $I_B = 1.5$ ma.		.90	Volts
C_{ie}	Emitter Capacitance	$I_C = 0$, $V_{EB} = 3V$, f = 1mc		5	pf
V_{OE}	Emitter Offset Voltage	$I_E = 0$, $I_B = 1.5$ ma.		2.5	MV
r_s	Saturation Resistance	$I_E = 0$, $I_B = 1.5$ ma.		15	Ohms

APPENDIX IV

CORROSION PROTECTION OF PLATED WIRES

TECHNICAL REPORT NO. 67

TITLE: CORROSION PROTECTION OF PLATED WIRES

ENGINEER: A. L. Salamon

PROJECT: 258

CONTRACT: NAS 5-9518

UNIT: Advanced Memories

DATE: August 3, 1965

ABSTRACT:

This report discusses methods which were tried to provide corrosion protection of plated wire memory elements. It was found that the Nickel-Iron magnetic film possesses, by itself, sufficient corrosion resistance when used inside the H-film-teflon tunnel structure, provided the surface is carefully cleaned. Wires resisted corrosion successfully after a maximum of 1417 hours at 95°C and 85% relative humidity.

Written by: A. L. Salamon
A. L. Salamon

Approved by: G. A. Fedde
G. A. Fedde

jam

A method of protective overplating was tried using relatively inert metals such as Tin, Gold, Rhodium, and Cadmium to protect the magnetic film from corrosion. For several reasons, enumerated below, this method of corrosion protection proved inadequate.

Reasons for failure of overplating approach:

1) In testing the wires for electrical performance mercury cups are used to make electrical contact with the wires. It was found that the protective coating, particularly the gold and tin, dissolve in the mercury and are removed completely or partially from the wire. It was found that a coating thus damaged caused faster corrosion than if no protection were used at all. Since the use of mercury contacts cannot be eliminated from the test set up this problem, by itself, precludes the use of Tin or Gold overplating.

2) Due to the effect of bimetallic couples in increasing corrosion rate it is imperative that when a plating of a metal more inert than the Fe-Ni of the magnetic plating is used there be no pinholes in the plating. If there is a pinhole, the two metals exposed to the corrosive medium form an electric cell of such a polarity that the more active Fe-Ni plating dissolves.

3) In order to produce a plating free from pinholes the protective metal had to be plated to a significant thickness ($> 10{,}000$ Å) but at this thickness the plating acted as an eddy-current shield and drastically reduced the magnetic output of the wires.

Many tests were run using various plating materials and plating methods but in each case significant corrosion was observed after a few hundred hours. In comparison, unplated control wires always showed slightly less corrosion. In all these tests wires were exposed to an environment of +95°C and 80% - 85% relative humidity. The wires were not protected by the H-film-Teflon tunnel structure which will actually be used in the memory.

Since the unprotected control wires showed less corrosion and since in actual practice the wires will be inside the protective tunnels it was thought worthwhile to study unprotected wires to see if by proper cleaning or surface conditioning they could resist corrosion.

At first the results were discouraging, but it was found that this was due to the fact that the temperature-humidity chamber used impure water which had a pH of 8.9. By switching to a pure de-ionized water of pH 6.4 corrosion was dramatically reduced.

A. L. Salamon
Whitpain
August 3, 1965

Three batches of wires were tested for 979, 1417 and 981 hours respectively at 95°C and 85% relative humidity. The first batch was not cleaned at all and after 979 hours the wires were in good to fair condition.

The purpose of the second batch was to see what effect the initial condition of the plating and cleaning had on corrosion rate. Half of the wires came from a batch which had porous plating with many flaws, and the other half came from a batch with excellent quality of plating. Some of each type were carefully cleaned by wiping with a tissue soaked in alcohol, the rest were purposely handled with the fingers to get them greasy and dirty. After 1417 hours all of the cleaned wires looked as good as new while the rest of the wires showed some corrosion but were still good to fair. No correlation was observed between corrosion rate and initial condition of the plating.

The third batch of wires was to test various methods of cleaning and to test the effect of silicone grease on reducing corrosion. It was found that the most effective method of cleaning was to wipe the wires with a tissue soaked in alcohol. If instead of wiping, the wires are soaked in alcohol (even if followed by an OAKITE and water rinse) corrosion was observed at one end of the wire indicating that impurities were concentrated there by the alcohol as the wire was held vertically. It was found that if the wires are wiped with alcohol additional cleaning in an oakite solution does not further help in preventing corrosion.

Silicone grease greatly reduces corrosion outside of the tunnel structure, but inside the tunnels it has practically no effect. (Actually, a very slight increase in corrosion was noted.) Cleaning of the wires is still important if silicone grease is used.

Although there are definite differences in the wires depending on cleaning, even the worst wires in this batch looked good after 981 hours at the environment.

On all wires in all batches, except those with silicone coating, corrosion outside of the tunnels was about 10 times greater (by percentage of corroded area) than inside. Corrosion penetrated about 1/8 to 1/4" in from the edge of the tunnel structure.

CONCLUSION:

The excellent results obtained on the unprotected wires indicates that with proper cleaning there should be no corrosion problems even though bare, unprotected wires are used.

A. L. Salamon
Whitpain
August 3, 1965

APPENDIX V

MATERIALS REPORT NUMBER ONE

MATERIAIS REPORT #1

MINIATURE SPACEBORNE MEMORY

Contract No. NAS5-9518

Prepared by: R. W. Hoffman

Approved by: G. R. Reid

1.0 SUBJECT

Materials Report #1

2.0 PURPOSE

The purpose of this report is to describe in summary form those tests, experiments, developments, and studies thus far performed and which are pertinent to material selection for use in fulfilling the technical requirements of this contract.

3.0 SUMMARY

3.1 After reviewing the environmental specifications invoked on the memory system, it was decided to tentatively select materials based on their ability to withstand the sterilization condition of 150°C for 48 hours. After a material has successfully withstood this condition, it would then be subjected to the other environments.

3.2 Materials used on this contract fall categorically into groups which comprise the individual subassemblies of the memory package. The subassemblies are: the active memory plane, the substrates and spacers, and the mechanical structure.

3.3 The following is a list of the materials tentatively selected to comprise the individual subassemblies.

3.3.1 Memory Plane

a. Base, Laminate
Kapton Polyimide Film - Type H

E. I. DuPont DeNemours & Co.
Film Department
Wilmington, Delaware

b. Word Line, Etched
Shield Mu 30

Magnetic Metals Co.
Camden, New Jersey

c. Cable, Plated Wire Carrier
Kapton, type HF

Kent Co.
Princeton, New Jersey

d. Ground,
Copper, Electrolytic Type

Anaconda American Brass Co.
Philadelphia, Pa.

e. Adhesive Film, Word Line Laminate
Type FM 1041R

Bloomingdale Rubber Co.
Havre De Grace, Maryland

f. Adhesive Film, General Bonding
Type FM 1044R

Bloomingdale Rubber Co.
Havre De Grace, Maryland

3.3.2 Substrates and Spacers

a. Facing, Substrate
Copper, Electrolytic Type

Anaconda American Brass Co.
Philadelphia, Pa.

b. Facing, Spacer
Kapton Polyimide Film - Type H

E. I. DuPont De Nemours & Co.
Wilmington, Delaware

c. Frame
Aluminum Alloy, Type 2024-T3

Alcoa Aluminum
Philadelphia, Pa.

d. Honeycomb Hobe
Aluminum Alloy, Type 5052

Hexcel Products, Inc.
Havre De Grace, Maryland

e. Adhesive
Type HT432 Film Adhesive

Bloomingdale Rubber Co.
Havre De Grace, Maryland

f. Support, Plated Wire, Molded
Type DEN 438 & DER 330 Blend

Dow Chemical Company
Camden, New Jersey

3.3.3 Mechanical Structure

a. Container, External
Aluminum Alloy, Type 6061T4

Aluminum Company of America
Philadelphia, Pa.

b. Structure, Support, Internal
Aluminum Alloy, Type 5052-T3

Aluminum Company of America
Philadelphia, Pa.

c. Hardware
Corrosion Resistant Steel
per QQ-S-763

4.0 GENERAL CONSTRUCTION AND LAYOUT

Enclosed in the appendix of this report is SK1006 which describes the general layout and construction of one-half of the 2.8 megabit memory system. Clearly outlined in the layout is the outside configuration and the general allocation of volume for the various active subsystems which when combined, form the entire memory stack. Detailed construction of each subsystem is contained in subsequent sections of this report.

5.0 ENVIRONMENT, MATERIAL

5.1 The following is a list of the applicable environments which the materials must withstand to be compatible with Article II, Specifications, Contract NAS5-9518.

5.2 Specifications, Environmental

a. Non-degrading operation oven temperature range of minus (-) 20°C to plus (+) 80°C.

b. Non-degraded operation after storage at plus (+) 150°C for 48 hours.

c. Non-degrading operation at 10^{-11} mm of Hf pressure or less.

d. Non-degrading operation at 100% R.H. with resulting condensation of water or frost.

5.3 After reviewing the above specifications, it is apparent that the most difficult one to meet is 5.2,b. (150°C for 48 hours). With due respect to the other specifications, it was determined that materials would be tentatively selected on the basis of their ability to meet this environment. After materials meet this condition, they would subsequently be exposed to the other environments.

6.0 MEMORY PLANE CONSTRUCTION

6.1 The memory plane consists basically of two items: the plated wire (contained in a cable), and the word line overlay. These two items are bonded together to form a 90° matrix in two parallel adjacent planes. The memory plane is then bonded to a ground plane, described in paragraph 7.0.

6.2 The bonding is accomplished at 350°F and 300 psi for one hour utilizing the film adhesive FM1044R, paragraph 3.3.1-f. Conventional techniques for high pressure bonding were utilized.

6.3 The memory plane described has been subjected to the 150°C ambient condition for time in excess of 48 hours. No detrimental effects on the plane were apparent after exposure tc this environment.

6.4 Plated Wire Cable

6.4.1 The plated wires must necessarily be contained in material which, with wires in place, cannot induce any stress or strain into the plated wire. A rather unique cable was used for this purpose.

6.4.2 The cable consists of two sheets of Kapton Type HF which have been fused together, FEP to FEP, with monel wires being encapsulated in the FEP. The monel wires are pulled out of the cable thus producing a series of parallel tunnels. The sense wires (plated wires) are then inserted into these tunnels and thus are physically protected and alligned with respect to the word line overlay.

6.4.3 A sample of the cable was prepared and bonded to a thick (.12 inch) copper clad glass epoxy laminate. Twenty polyurethane insulated plated wires were inserted in the tunnels of the cable. The material was subjected to the following: temperature cycling (10 cycles, 1 hour per cycle) between 0°F and (+) 140°F, soak four days at (+) 75°C, soak three days at (-)20°C, soak +150°C three days and finally, soaked at 190°C for seventeen days. All insulated plated wires were free in the tunnelled cable and the bond between the cable and the copper retained its strength.

6.5 Word Line Overlay

The word line overlay is basically a group of word lines etched from the word line laminate. The conventional resist and etch method was utilized to produce the lines. Kodak Photo Resist was utilized with the laminate being etched with ferric chloride.

6.5.1 Laminate, Word Line

The word line laminate is a composite of "H" film, adhesive, and Shield Mu 30, which is subsequently copper plated on the out side surface after bonding takes place. This laminate is fabricated in house because it is not purchasable from commercial laminate suppliers except on special order. The composite is bonded at 650 psi, 350°F for one hour between two ground metal platens.

6.5.1.1 "H" Film Base

The film "H film" was selected as the base material for all word line laminates. It was selected for its high temperature stability and mechanical strength. At 150°C the material exhibited no deteriorization and bonded extremely well to the adhesive "FM1044R". A data sheet is contained in the appendix.

6.5.1.2 An attempt to use a glass epoxy laminate type FR4 was made. When this laminate (.002" thick) was subjected to the 150°C environment, extreme charring and warping of the epoxy resin was apparent after a short period of time. The exposure lasted 60 hrs. and resulted in a completely charred overlay with radical deformations apparent in the copper word lines.

6.5.1.3 Adhesive

Conferring with the Bloomingdale Rubber Co., Havre De Grace, Maryland, it was determined that the vendor's product "FM1041R Film Adhesive" would withstand the temperature requirements of "MIL-A-25463, Type II, Adhesive". The adhesive was obtained and laminates bonded together to form the memory's word line structure. The samples were then subjected to a 150°C environment for 60 hours with no deterioration apparent. The adhesive was then tentatively approved for application on this program.

6.5.1.4 Word Lines

From an electrical standpoint, shielded copper word lines were selected for this memory application. The word lines are etched from a copper plated, shield Mu 30, clad "H" film laminate. The shield Mu 30 is an 80% nickel-iron alloy.

7.0 SUBSTRATE AND SPACER CONSTRUCTION

7.1 The substrate and spacer are both honeycomb structures. The substrate is utilized for a spacer, mechanical support, and ground plane between active memory planes. It contains conductive metallic surfaces which are bonded to the outside surfaces of an aluminum frame containing aluminum honeycomb. The facing (copper, gold plated) is bonded to the frame utilizing an epoxy-phenolic, aluminum filled, glass cloth base, film adhesive. The adhesive material is designated "HT-432" per Bloomingdale Rubber Co., Havre De Grace, Maryland.

7.2 The spacer construction is similar to that of the substrate except that the facing utilized is both non-metallic and non-conductive. "H" film polyimide film will be used for this facing with the remainder of the construction similar to para. 7.1.

7.3 With respect to both constructions and material selections, a test report has been included in the appendix. This report, entitled "Qualitative Analysis of Memory Plane Substrate Structure, TTR-92454-1", details the composition of the substrate and the tests performed which led to the tentative material selections indicated.

8.0 GENERAL MECHANICAL STRUCTURE

8.1 The internal structure as well as the external case will be fabricated from aluminum alloy. All internal structures will be fabricated from type 5052-T4 and will contain an iridite finish.

8.2 The external case will be fabricated from type 6061-T4 and will be finished with an iridite inside and black anodize outside.

8.3 The above materials and finishes are widely utilized throughout the satellite industry and black boxes similar to this unit have been tested in satellites such as Ranger, Tiros and Lunar Orbitor.

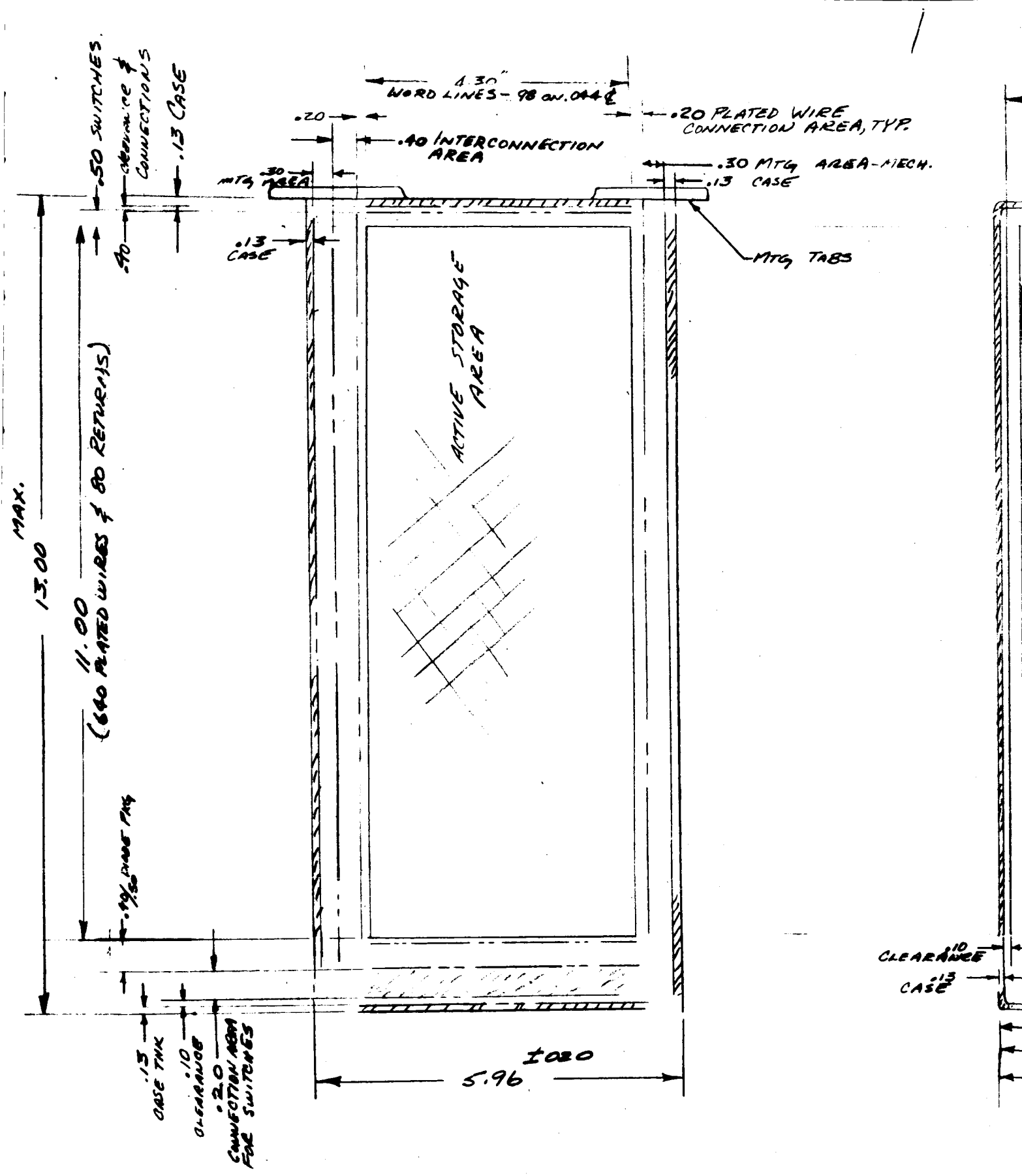
9.0 FUTURE EVALUATION

9.1 Since all materials have been tentatively selected on their ability to withstand the thermal environment, they must all be subjected to the other specified environments. Samples of the planes will be fabricated and will be subjected to the other conditions. The results of these tests will certify the tentative selections.

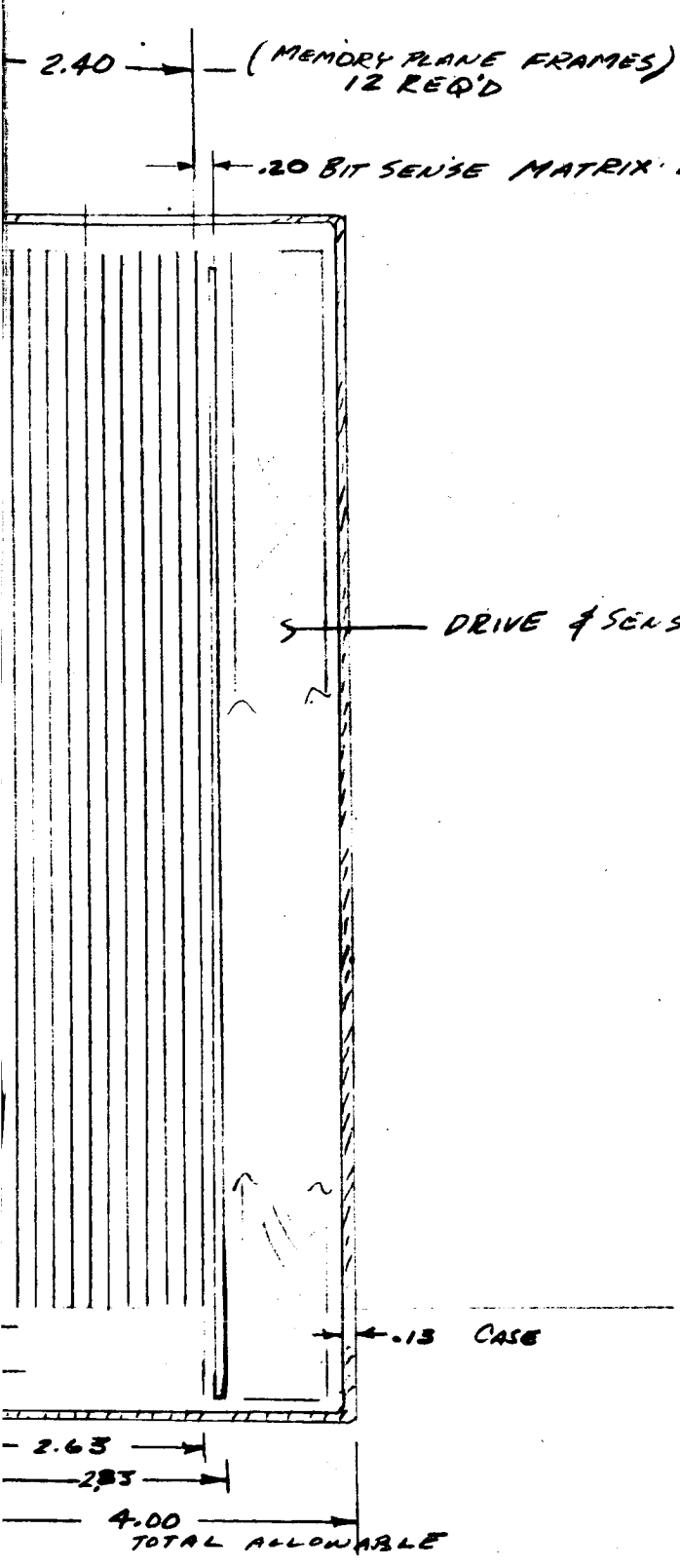
9.2 Where materials break down in the other test conditions, they will be re-evaluated and other materials will be subsequently investigated and tested.

9.3 When all materials are thoroughly certified, a final material report will be issued.

A P P E N D I X


4.30"
WORD LINES - 98 ON .044 ℄
.20
.20 PLATED WIRE CONNECTION AREA, TYP.
.40 INTERCONNECTION AREA
.30 MTG AREA - MECH.
.13 CASE
MTG TABS
.30 MTG AREA
.13 CASE
.50 SWITCHES
.40 INTERCONNECTION & CONNECTIONS
.13 CASE
.40
MAX. 13.00
11.00
(640 PLATED WIRES & 80 RETURNS)
ACTIVE STORAGE AREA
.10 CLEARANCE
.13 CASE
.13 CASE TNK
.10 CLEARANCE
.20 CONNECTION AREA FOR SWITCHES
5.96
1020

2

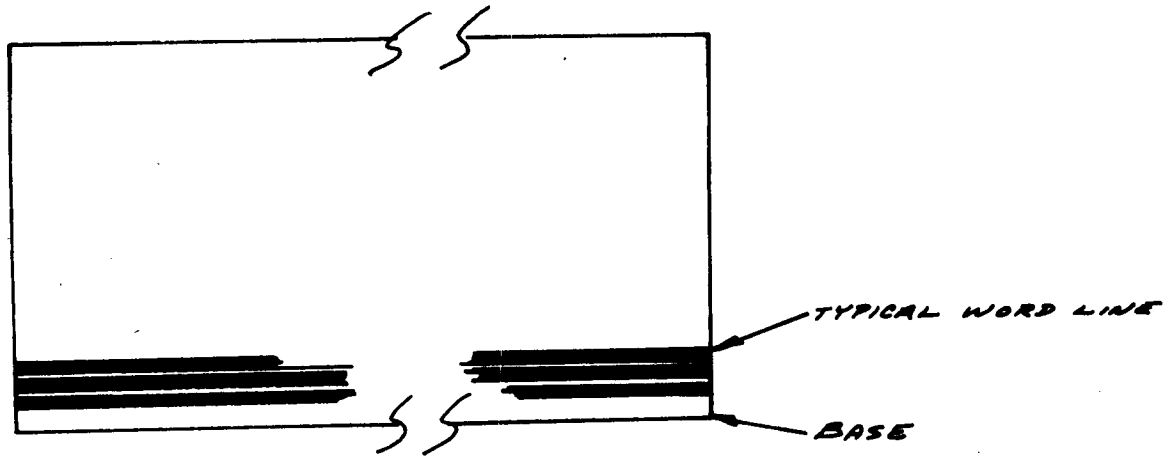


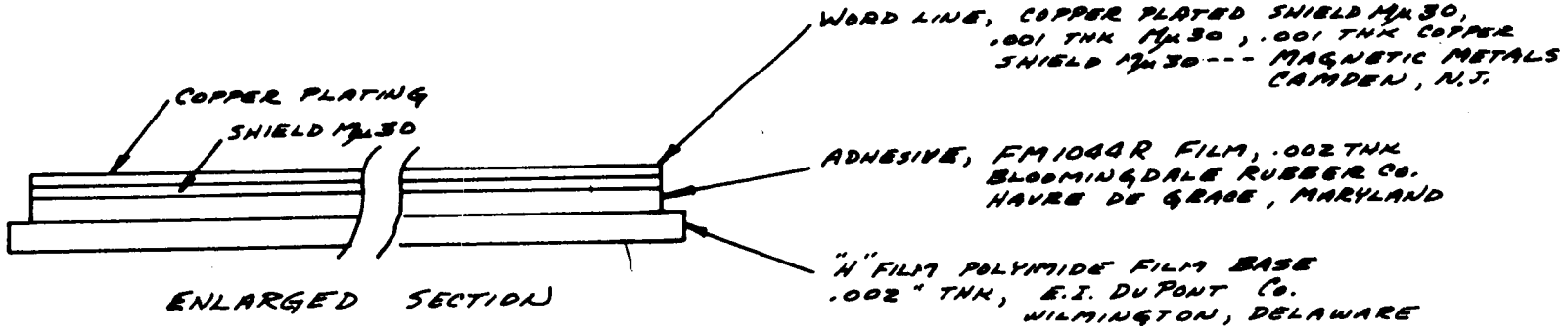
NOTES:
1- CASE MATERIAL: ALUM. ALLOY
TYPE 6061 T4

MEMORY STACK

R W Holton 1-14-65

SK 1006





ENLARGED SECTION

NOTE: ALL LAMINATES ARE BONDED AT 600 PSI, 350°F, FOR 1 HR.

LAMINATE

MEMORY PLANE

R.W. Hoffman
6-12-65

SK # AP1080

DU PONT

H FILM

polyimide film

BULLETIN H-1

SUMMARY OF PROPERTIES

SUMMARY OF PROPERTIES

GENERAL

H Film is a polyimide, resulting from the polycondensation reaction between an aromatic tetrabasic acid and an aromatic diamine. Its ability to maintain its excellent physical, electrical and mechanical properties over a wide temperature range has opened new design and application areas to film technology. This is especially true in applications which have high operating temperatures.

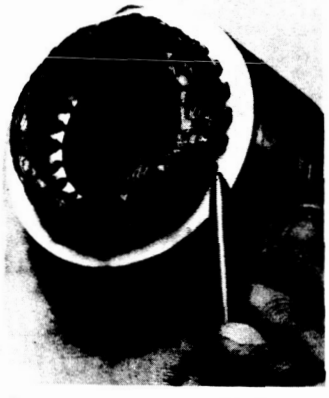
H Film has been used successfully in applications where the temperatures have been as low as −269°C. and as high as 400°C. At room temperature, the properties of "Mylar"* polyester film and H Film are similar. However, as the temperature is increased or decreased the properties of H Film are less affected than those of "Mylar". A flame resistant material, H Film begins to char above 800°C. There is no known organic solvent for the film and it is infusible and does not melt.

Because H Film had no melting point, Du Pont combined "Teflon"* FEP-fluorocarbon resin with the polyimide to give a heat sealable structure for fabrication purposes. (See Bulletin HF-1 for details)

Finished articles may also be made by the use of adhesives which are available for bonding H Film to itself, to metals, to papers of various types and to other films. H Film can also be laminated, metalized, punched, formed or adhesive coated.

Applications for H Film include: wire and cable wrap, motor slot liners, formed coil wrap, transformers, capacitors, flexible printed circuits, magnetic and pressure sensitive tapes, and hose and tubing. Many of these applications are based on the fact that its electrical properties, such as dielectric strength and dissipation factor, are excellent and remain nearly constant over a wide range of temperature and frequency. Others make use of its radiation resistance or chemical resistance at elevated temperatures. It is this combination of useful properties at extremes in temperatures which make H Film a unique, new industrial material.

*Du Pont registered trademark



Precision motors use slot liners made of H film because of the material's toughness and its ability to insulate at higher operating temperatures.

H Film is a transparent gold colored film which can be run on conventional film handling equipment with little if any adjustment.

H film finds use as layer insulation in transformers. The polyimide insulation permits the design of smaller units which operate at higher temperatures with no reduction in rating.

Printed circuits and flat cable constructions have been made from H Film because of its dimensional stability at high temperature and its solder resistance. H Film is used as a wire wrap where good high temperature insulation and low weight structures are required.

SUMMARY OF PROPERTIES OF H-FILM

PROPERTY		TYPICAL VALUES			TEST METHOD
		−195°C	25°C	200°C	
PHYSICAL PROPERTIES					
Ultimate Tensile Strength	(MD)	35,000 psi	25,000 psi	17,000 psi	ASTM D-882-61T
Yield Point	(MD)		10,000 psi at 3%	6,000 psi at 3%	ASTM D-882-61T
Stress to Produce 5% Elongation	(MD)		13,000 psi		ASTM D-882-61T
Ultimate Elongation	(MD)	2%	70%	90%	ASTM D-882-61T
Tensile Modulus	(MD)	510,000 psi	430,000 psi	260,000 psi	ASTM D-882-61T
Impact Strength			6 Kg-cm/mil		Du Pont Pneumatic Impact Test
Folding Endurance (MIT)			10,000 cycles		ASTM D-643-43
Tear Strength—Propagating (Elmendorf)			8 gm/mil		ASTM D-1922-61T
Tear Strength—Initial (Graves)			510 gm/mil		ASTM D-1004-59T
Bursting Test (Mullen)			75 psi		ASTM D-774-46
Density			1.42 gm/cc		ASTM D-1505-57T
Coefficient of Friction Kinetic (Film-to-Film)			.42		ASTM D-1894-61T
Refractive Index (Becke Line)			1.78		Encyclopaedic Dictionary of Physics, Volume I
Area Factor			135 ft^2/lb./mil		Calculation

PROPERTY	TYPICAL VALUES				TEST CONDITION	TEST METHOD
THERMAL PROPERTIES						
Melting Point	NONE					
Zero Strength Temperature	815°C				20 psi load for 5 seconds	Hot Bar (Du Pont Test)
Cut-through Temperature	435°C					Weighted Probe on Heated Film (Du Pont Test)
Coefficient of Linear Expansion	2.0×10^{-5} in./in./°C				(—) 14°C to 38°C	ASTM D-696-44
Coefficient of Thermal Conductivity	3.72×10^{-4} $\frac{(cal)(cm)}{(cm^2)(sec)(°C)}$ 3.89×10^{-4} " 4.26×10^{-4} " 4.51×10^{-4} "				25°C 75°C 200°C 300°C	Model TC-1000 Twin Heatmeter Comparative Tester
Flammability	Self-extinguishing					
Heat Sealable	No					
	250°C	275°C	300°C	400°C		
Shrinkage	0.3%		0.5%	3.5%	30 minutes	ASTM D-1204
Heat Aging (In air)	8 yrs.	1 yr.	3 months	12 hours		Time to Reach 1% Elongation

H-FILM — A USEFUL FILM FROM -269°C to 400°C

PROPERTY	TYPICAL VALUES % Tensile Retained	% Elongation Retained	% Modulus Retained	TEST CONDITION	TEST METHOD
CHEMICAL PROPERTIES				Days Immersed at Room Tempertaure	
CHEMICAL RESISTANCE TO:					
Benzene	100	82	100	365	
Toluene	94	66	97	365	
Methanol	100	73	140	365	
Acetone	67	62	160	365	
10% Sodium Hydroxide		Degrades		5	
Glacial Acetic Acid	85	62	102	36 days at 110°C	
p-Cresol	100	77	102	22 days at 200°C	
"Arochlor" *	100	53	142	365 days at 200°C	
Transformer Oil	100	100	100	180 days at 150°C	
Water pH = 1	65	30	100	14 days at 100°C	
pH = 4.2	65	30	100	14 days at 100°C	
pH = 7.0	65	30	100	70 days at 100°C	
pH = 8.9	65	20	100	14 days at 100°C	
pH = 10.0	60	10	100	4 days at 100°C	
RADIATION RESISTANCE					
Gamma (Savannah River)	Still Flexible (180° Bend)			Exposure 4.16 x 10^8 RADS	
Electron (Van der Graff)	Retains 50% of Original Elongation			Exposure 6 x 10^8 RADS	
Neutron plus Gamma (Brookhaven)	Darkened but tough			Exposure 10^{10} RADS	
UV	Excellent				Westinghouse Fluorescent Sunlamps Ozone Present, Dry Environment
FUNGUS RESISTANCE	Inert			12 months	Soil Burial
MOISTURE ABSORPTION	1.3% 2.9%			50% Relative Humidity at 23.5°C Immersion for 24 hrs. at 23.5°C	Constant Environment Room ASTM D-570-59T
HYGROSCOPIC COEFFICIENT OF EXPANSION	2.2 x 10^{-5} in/in/% Relative Humidity			72°F 20% - 80% Relative Humidity	
PERMEABILITY					
Gas	cc/(100 in²) (24 hrs.) (atm/mil)			23°C	ASTM D-1434-58
Carbon Dioxide	45				
Hydrogen	250				
Nitrogen	6				
Oxygen	25				
Helium	415				
Water Vapor	gm/(100 in²) (24 hrs.)/mil 5.4				ASTM E-96-53T

PROPERTY	TYPICAL VALUES −195°C	25°C	200°C	TEST CONDITION	TEST METHOD
ELECTRICAL PROPERTIES					
Dielectric Strength (1-mil)	10,800	7,000 volts	5,600 volts	60 cycles	ASTM D-149-61
Dielectric Constant		3.5	3.0	1 kilocycle	ASTM D-150-59T
Dissipation Factor		.003	.002	1 kilocycle	ASTM D-150-59T
Volume Resistivity		10^{16} ohm-cm	10^{14} ohm-cm		ASTM D-257-61
Surface Resistivity		10^{16} ohms		50% Relative Humidity	ASTM D-257-61
Corona Start Voltage (1-mil)		465 volts		50% Relative Humidity	ASTM D-1868-61T
Insulation Resistance		100,000 megohm mfds.		100°C	Based on 0.05 mfd. wound capacitor using 1-mil H Film

*Monsanto registered trademark

SUPPLY OF H FILM

Only experimental quantities of H Film in 1, 2, 3 and 5 mil gauges and a maximum width of 18 inches are available at this time. These films are made in our laboratory semiworks at Buffalo, New York. Larger widths will become available when our prototype plant comes on stream in 1965.

Requests for the film and any questions concerning the use, properties, etc., of H Film will be handled most rapidly by addressing your inquiry to:

Venture Development Section
Film Department
E. I. DU PONT DE NEMOURS & COMPANY (Inc.)
Wilmington, Delaware 19898

Our experimental designations for H Film are as follows:

Du Pont Designation	Nominal Guage	Approximate Yield (sq. ft. 1 lb.)
100-XH-667	1 mil	135
200-XH-667	2 mil	67.5
300-XH-667	3 mil	45
500-XH-667	5 mil	27

The first three digits of the experimental designation refer to the gauge of the film. "X" means experimental and "H" means polyimide film. The last three digits are for internal identification purposes.

QUALITATIVE ANALYSIS OF MEMORY PLANE SUBSTRATE STRUCTURE

TTR-92454-1

(ADDENDUM)

MINIATURE SPACEBORNE MEMORY

Prepared by: R. W. Hoffman

Approved by: G. R. Reid

ac
7/7/65

1.0 SUBJECT: Addendum

Qualitative analysis of memory plane substrate structure. TTR-92454

2.0 PURPOSE:

The purpose of this addendum is to update the report dated March 5, 1965.

3.0 SUMMARY:

3.1 Referring to paragraph 3.2 of the original report, the adhesive film to be utilized for the bonding of facings to honeycomb was tentatively selected. That adhesive was HT424, a film type, supplied by the Bloomingdale Rubber Co., Havre De Grace, Maryland.

3.2 Subsequent tests indicate that another adhesive, HT432 also a film type, from the same vendor provided a much more uniform bond strength. The difference between the two adhesives is that HT432 contains a closely woven glass cloth fabric carrier whereas HT424 contains a coarsely woven glass cloth carrier. The finer weave spreads the resin more uniformly, thus producing a voidless uniform glue line.

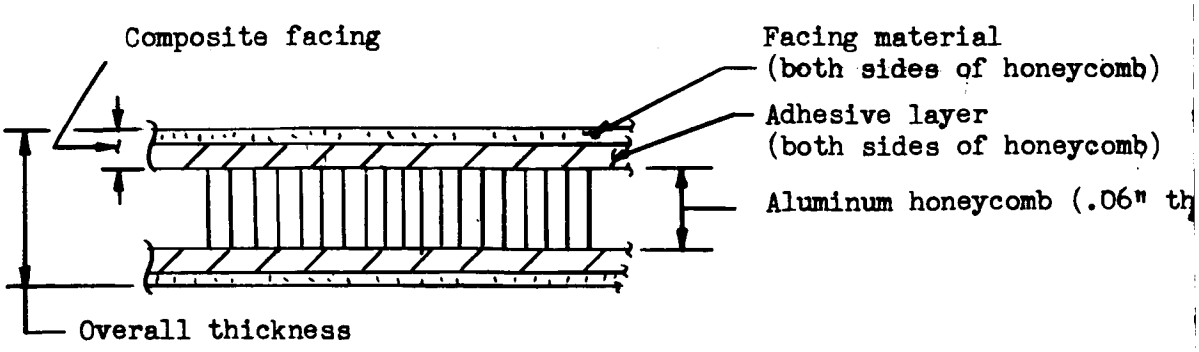
4.0 SAMPLE, TEST

4.1 The test sample was fabricated utilizing 3 oz. copper facings (2 req'd), adhesive (HT432), and aluminum honeycomb hobe per paragraph 5.1.1. The composite was bonded between metal platens at 350°F and 200 psi pressure for one hour. When the sample was removed from the press, it exhibited no physical deformation or material degradation. The bond strength was extremely high.

4.2 The sample was then placed in an ambient of 150°C for 64 hours. After cooling, the sample was examined and showed no material degradation, and the adhesive strength was similar to that of the sample prior to sterilization.

4.0 SUBSTRATE CONSTRUCTION

4.1 The following diagram deliniates a typical substrate cross section, with overall sizes ranging from 5.0" x 12.0". It should be noted that Chart 1 deliniates only the material layers on one side of the honeycomb.



TYPICAL SUBSTRATE STRUCTURE

4.2 All facing materials and adhesives are listed in Chart #1.

5.0 MATERIALS

5.1 Honeycomb

5.1.1 Aluminum Alloy Type 5052
.002" gauge, 1/8-5052-P
.39" web

Vendor: Hexcel Products, Inc.
Havre De Grace, Maryland

5.2 Facing

5.2.1 a) Copper Foil, Printed Circuit Grade, 1 oz.
b) Copper Foil, Printed Circuit Grade, 2 oz.
c) Copper Foil, Printed Circuit Grade, 3 oz.

Vendor: Anaconda American Brass Co.
Philadelphia, Pennsylvania

5.2.2 Shield Mμ 30, .004" thick stock, no coating

Vendor: Magnetic Metals, Inc.
Camden, New Jersey

5.2.3 Glass Epoxy Laminate, Copper Clad (1 oz.), .005 thick

Vendor: Precision Laminates
Danbury, Connecticut

5.3 Fillers and Support

5.3.1 a) Glass Cloth Fabric, .002" thick, no finish
b) Glass Cloth Fabric, .004" thick, no finish

5.4 Adhesives

5.4.1 Film

5.4.1.1 AF 202, .015" thick

Vendor: 3M Company
St. Paul, Minnesota

5.4.1.2 HT424, .015" thick

Vendor: Bloomingdale Rubber
Havre De Grace, Maryland

5.4.2 Liquid

5.4.2.1 DEN 438, Epoxy Novalac

Vendor: Dow Chemical Company
Midland, Michigan

1) NMA Hardener

Vendor: Allied Chemicals
Philadelphia, Pennsylvania

2) Polyamid Hardener

Vendor: Fluoro Plastics, Inc.
Philadelphia, Pennsylvania

5.4.2.2 HYSOL 2094, Printed Circuit Adhesive

Vendor: Hysol Corporation
Olean, New York

5.4.3 Microbond Bonding Sheets (Pre-Preg)

5.4.3.1 "B" Stage Glass Epoxy, .0055 & .0035" thick

Vendor: General Electric Company
Drexel Hill, Pennsylvania

6.0 QUALITATIVE DATA

6.1 Chart 1 of this report itemizes the various substrate constructions and adhesives utilized. This chart also provides detailed information with respect to adhesive formulations, special processes utilized, failure modes, and relative strengths obtained.

6.2 No attempt has been made to develop quantitative data for any specific substrate system. This type of information is not within the scope of this report. A quantitative analysis will be achieved at a future time.

CHART 1

ADHESIVE SYSTEM	ITEM	NO. OF LAYERS	LAMINATE COMPOSITION	TIME*	FAILURE MODE	COMMENTS
A - LIQUID 1 - Hysol 2094 & Pre-Preg	1	7	Copper foil, 1 oz. Pre-preg(.0055")(2) Honeycomb	48	Bond, adh. to honeycomb	Two layers of pre-preg utilized to increase resin thickness. Adhesion to copper foil good; however, blistering occurred between copper foil and honeycomb.
	2	9	Copper foil, 1 oz. Adhesive Pre-preg (.0055")(2) Honeycomb	48	Bond, pre-preg to honeycomb	Bond to copper foil increased compared to item 1. Blistering apparent between pre-preg and honeycomb.
	3	7	Clad G10, 1 oz. Pre-preg (.0035")(2) Honeycomb	48	Bond, pre-preg to honeycomb	Bond to G10 very good. Small blisters apparent between pre-preg and honeycomb.
	4	7	Copper foil (.001") Pre-preg (.0035")(2) Honeycomb	48	Bond, Pre-preg to honeycomb	Edges of laminate sealed with conductive epoxy to prevent oxidation of adhesive. Blistering still took place between pre-preg and honeycomb.
	5	7	Shield Mμ30 Pre-preg (.0055")(2) Honeycomb	48	Oxidation of pre-preg	Pre-preg edges oxidized. No separation of materials took place.
	6	9	Shield Mμ30 Adhesive Pre-preg (.0055")(2) Honeycomb	48	Oxidation of pre-preg	Pre-preg became oxidized. Bond strength lowered due to this condition.
	7	11	Copper foil Pre-preg (.0055") Shield Mμ30 Pre-preg (.0055")(2) Honeycomb	48	Bond, Pre-preg to honeycomb & Mμ30 to copper	Mμ30 laminated into structure to provide electrical shield. Each adhesive layer blistered.
	8	9	Copper plating (.001") Shield Mμ30 Adhesive Pre-preg (.0055)(2) Honeycomb	48	Oxidation of pre-preg	Oxidation of pre-preg apparent. Bond between pre-preg and honeycomb small. No blisters apparent.

* Time indicates hours in 150°C ambient.

CHART 1 (continued)

ADHESIVE SYSTEM	ITEM	NO. OF LAYERS	LAMINATE COMPOSITION	TIME*	FAILURE MODE	COMMENTS
1 - Continued	9	13	Copper foil, 1 oz. Adhesive Shield Mμ30 Adhesive Pre-preg (.0055")(2) Honeycomb	48	Bond, Copper to Mμ30; Mμ30 to honeycomb	Blistering took place at both adhesive layers.
	10	13	Copper foil, 1 oz. Adhesive Shield Mμ30 Adhesive Pre-preg (.0035")(2) Honeycomb	48	Bond, Pre-preg to honeycomb & Mμ30 to copper	Edges of laminate sealed with conductive Epoxy to prevent oxidation of adhesive. Blistering still took place at each adhesive layer.
	11	5	Pre-preg (.0055")(2) Honeycomb	48	Oxidation of pre-preg	Cured pre-preg was exposed to environment. Pre-preg oxidized completely and became very brittle but still exhibited some bond strength to honeycomb.

* Time indicates hours in 150°C ambient.

CHART 1 (continued)

ADHESIVE SYSTEM	ITEM	NO. OF LAYERS	LAMINATE COMPOSITION	TIME*	FAILURE MODE	COMMENTS
A-LIQUID						
2-DEN 438 W/NMA Hardener and DMP Catalyst	1	5	Shield Mu30 Adhesive Honeycomb	See Comments	Bond, Mu30 to Honeycomb	Adhesive "B" staged on Mu30. Was applied with 10-32 threaded rod. Unit then laminated at 330°C 2-hours. No bond obtained between honeycomb and foil.
	2	5	Copper foil, 1-oz. Adhesive Honeycomb	50	Bond, Foil to Honeycomb	Adhesive applied to foil with 10-32 threaded rod. M.E.K. was used as thinner. Laminate was formed using wet lay up. Sample cured at 302°F, 2-hours. No blistering apparent but bond strength extremely low.
	3	5	Same as above	50	Bond, Foil to Honeycomb	Adhesive not thinned. Results same as shown above, #2.
	4	5	Same as above	50	Bond, Foil to Honeycomb	Same as #3, except ratio of resin to hardener change from 1/1 to 2/1.
	5	5	Copper foil, 2-oz. Adhesive Honeycomb	48	Bond, Foil to Honeycomb	Formulation was: 100g-87.5gm-1.5g of Resin, hardener, catalyst, respectively. Adhesive "B" staged on honeycomb and copper foil. Results: no flow of adhesive apparent, resulted in low bond strength.
	6	7	Copper foil, 2-oz. Adhesive Glass cloth (.002") Honeycomb	48	Bond, Foil to Honeycomb	Formulation same as #5. Glass cloth (.002") impregnated with adhesive "B" staged on copper foil. Honeycomb "B" staged also. Results same as #5.
	7	5	Copper foil, 2-oz. Adhesive Honeycomb	48	Bond, Foil to Honeycomb	Adhesive formulation same as #5. Honeycomb "B" staged. Adhesive applied to copper foil then unit laminated in wet condition. Results: "B" stage did not flow and produced low bond strength.

* TIME indicates hours in 150°C ambient.

CHART 1 (continued)

ADHESIVE SYSTEM	ITEM	NO. OF LAYERS	LAMINATE COMPOSITION	TIME*	FAILURE MODE	COMMENTS
3 - DEN 438 & Polyamid Hardener	1	9	Copper foil (1 oz.) Adhesive Glass cloth (.002") Adhesive Honeycomb	64	Bond, glass cloth to honeycomb	Formulation: 70 parts DEN 438-EK 85 to 30 parts hardener. Wet layup utilized to increase wetting action. Results: bond failure to honeycomb. Facing exhibited cellular dimpling. Resin charred and brittle.
	2	9	Copper foil (1 oz.) Adhesive Glass Cloth (.004") Adhesive Honeycomb	64	Same as above	Same as above
	3	5	Copper plated Shield Mμ30 (.004") Adhesive Honeycomb	24	None	Formulation of 60-40% resin to hardener. Adhesive applied to shield Mμ and wet lay-up utilized. No apparent failure of sample except discoloration of adhesive.
	4	5	Gold plated Shield Mμ30 (.004) Adhesive Honeycomb	32	None	Formulation of 3 to 2 by weight of resin to hardener. No apparent failure except discoloration of adhesive.
	5	5	"H" Film, copper clad Adhesive Honeycomb	64	Bond	H film backing in copper was coated with adhesive G7-200. This adhesive broke down at 150°C.
	6	5	Copper foil, 1 oz. Adhesive Honeycomb	64	None	No apparent failure was noted. Edges of honeycomb were sealed with GE #112 Silicone Rubber compound so that no air could attach the adhesive.
	7	5	Copper foil, 2 oz. Adhesive Honeycomb	64	None	Same as #6.

*150°C ambient

CHART 1 (continued)

ADHESIVE SYSTEM	ITEM	NO. OF LAYERS	LAMINATE COMPOSITION	TIME*	FAILURE MODE	COMMENTS
B-FILM						
1-AF 202	1	5	Copper foil, 2-oz. Adhesive Honeycomb	48	Bond Honeycomb to Adhesive	Units prior to exposure to environment were uniform in appearance and of good quality. After exposure, adhesive completely delaminated from honeycomb.
	2	5	Copper foil, 1-oz. Adhesive Honeycomb	48	Bond Honeycomb to Adhesive	Same as #1. There was no apparent difference in results by varying foil thicknesses.
2-HT 424	1	5	Copper foil, 3-oz. Adhesive Honeycomb	54	None	No detrimental effects apparent. Laminate remained flat and straight throughout exposure to 150°C ambient. When flexed, composite does take a set.
	2	5	Copper foil, 1-oz. Adhesive Honeycomb	64	None	Same as #1, except some dimpling apparent.

* TIME indicates hours in 150°C ambient.

QUALITATIVE ANALYSIS OF MEMORY PLANE SUBSTRATE STRUCTURE

TTR-92454-1

MINIATURE SPACEBORNE MEMORY

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Approved by: G. R. Reid

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3/5/65

1.0 SUBJECT: Qualitative Analysis of Memory Plane Substrate Structure.

2.0 PURPOSE:

2.1 The purpose of this analysis is to determine the acceptability of various substrate structures and adhesives for use in conjunction with the Miniature Space Borne Memory System.

2.2 The acceptability was based on mechanical structure and ability to withstand an invoked environment of storage at 150°C for 48-hours. This environment was assumed to provide the most detrimental effects on substrate materials.

3.0 SUMMARY:

3.1 In order to attain a minimum weight, the substrate was fabricated from aluminum honeycomb (1/16-inch thick nom.) with various facing materials bonded to it. The honeycomb was chosen for a structural spacer because of its high strength to weight ratio.

3.2 The substrate exhibiting the most favorable characteristics was composed of five layers of material as follows: Electrolytic copper foil (.0045-inch thick), adhesive film (.015-inch thick, HT424, Bloomingdale Rubber), aluminum honeycomb, adhesive film and copper foil. The sample size was approximately 5" x 5" and .072-inch thick after cure. This sample was placed in a 150°C ambient for 54-hours and visually exhibited no apparent deterioration. The weakest bond in this system was the foil to the adhesive bond. In addition, the adhesive could not readily be removed from the honeycomb.

3.3 In addition to the above mentioned composite, the DEN438 resin containing the polyamid hardener was also acceptable. However, the liquid system is much more difficult to use and provides a much lower bond strength.

3.4 The HT424 adhesive will be tentatively adopted for all honeycomb structure laminating on this program.

3.5 Quantitative tests will now be performed on honeycomb samples bonded with HT424. These tests will indicate strength levels obtained by: varying the adhesive thickness, varying the filler content, and subjecting the samples to other environments. The weight of the various samples will also be a contributing factor in the final decision as to which composite is the most acceptable for space borne memory applications.